Welcome To

ISSCC 2014
Session 26
Energy-Efficient Dense Interconnect

A 130mW 20Gb/s Half-Duplex Serial Link in 28nm CMOS

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Outline

- Motivation
- Transceiver Architecture
- Clocking
- Transmitter
- Receiver
- Receiver Adaptation
- Silicon Results
- Conclusion

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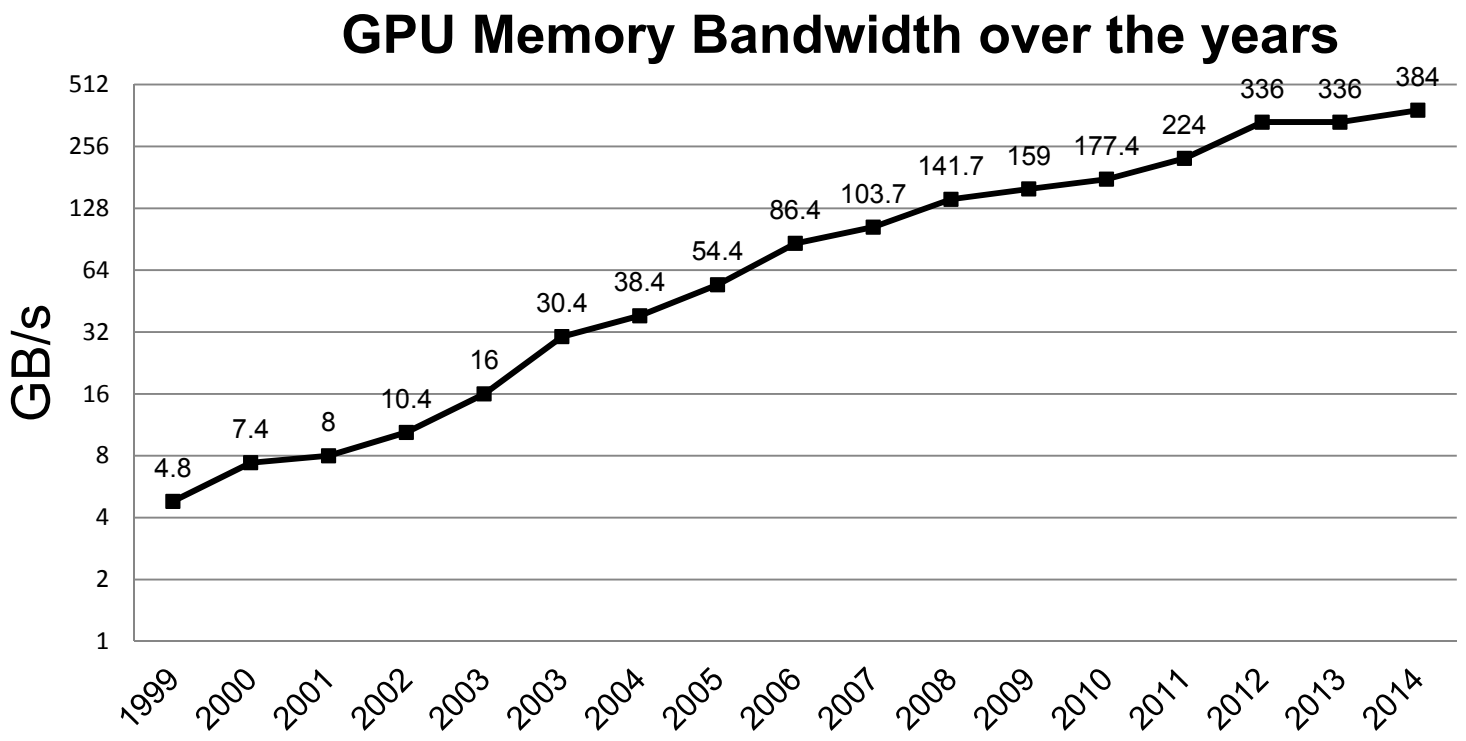
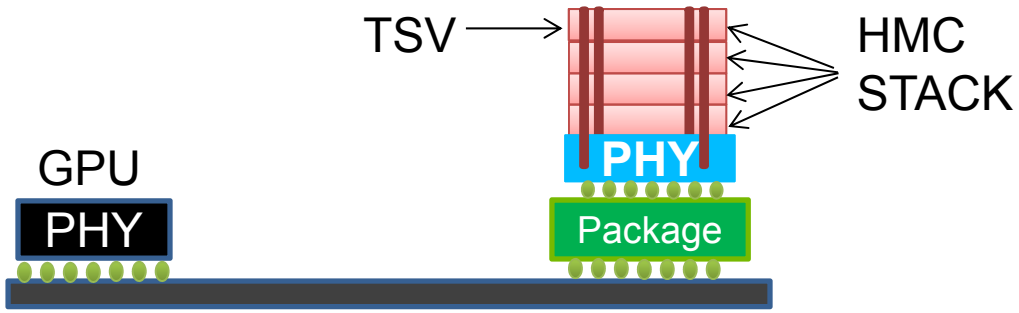
Motivation





Architecture Requirement

- Suitable for MCM and off-package signaling
- Power Efficiency
- Very low latency
- Insertion loss of 20dB or better
- Bandwidth per perimeter (Gbps/um)
- Throughput (Gbps/pin)
- BER < 10^{-18}
- Robust adaptation loops

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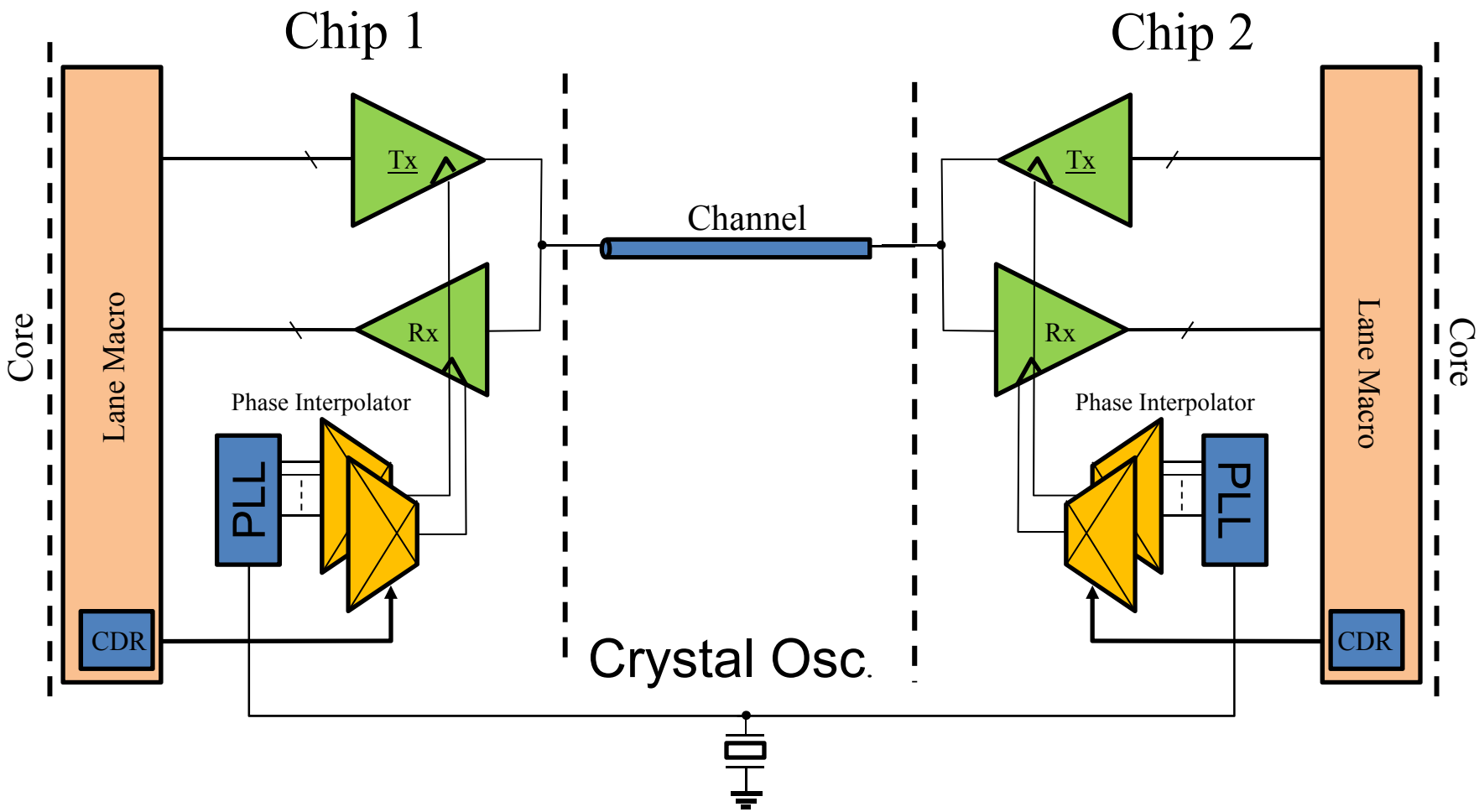
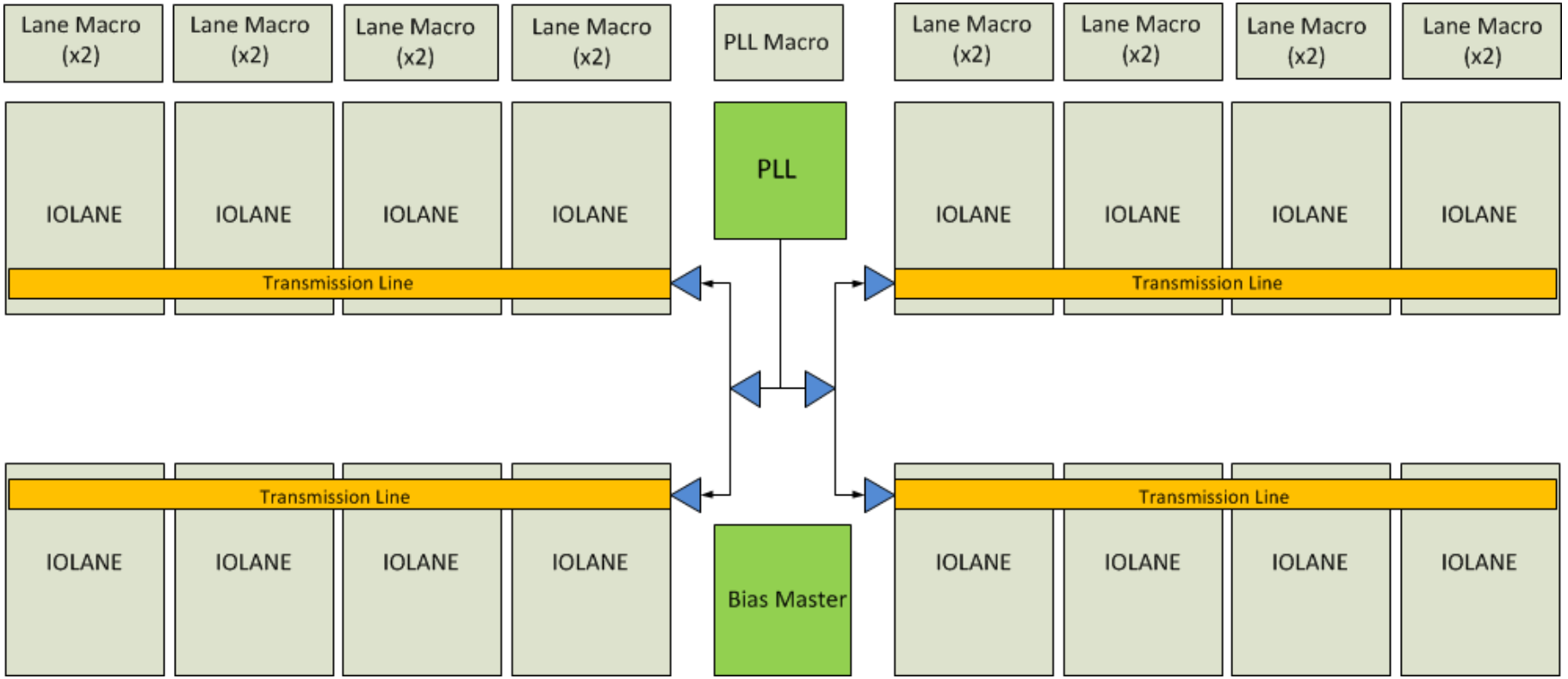
Half-duplex Transceiver



- Half-Duplex design to maximize BW per IO
- Differential signaling

IOBrick



- Common PLL frequency synthesis and bias generation
- IOLANE consist of the half-duplex transceiver

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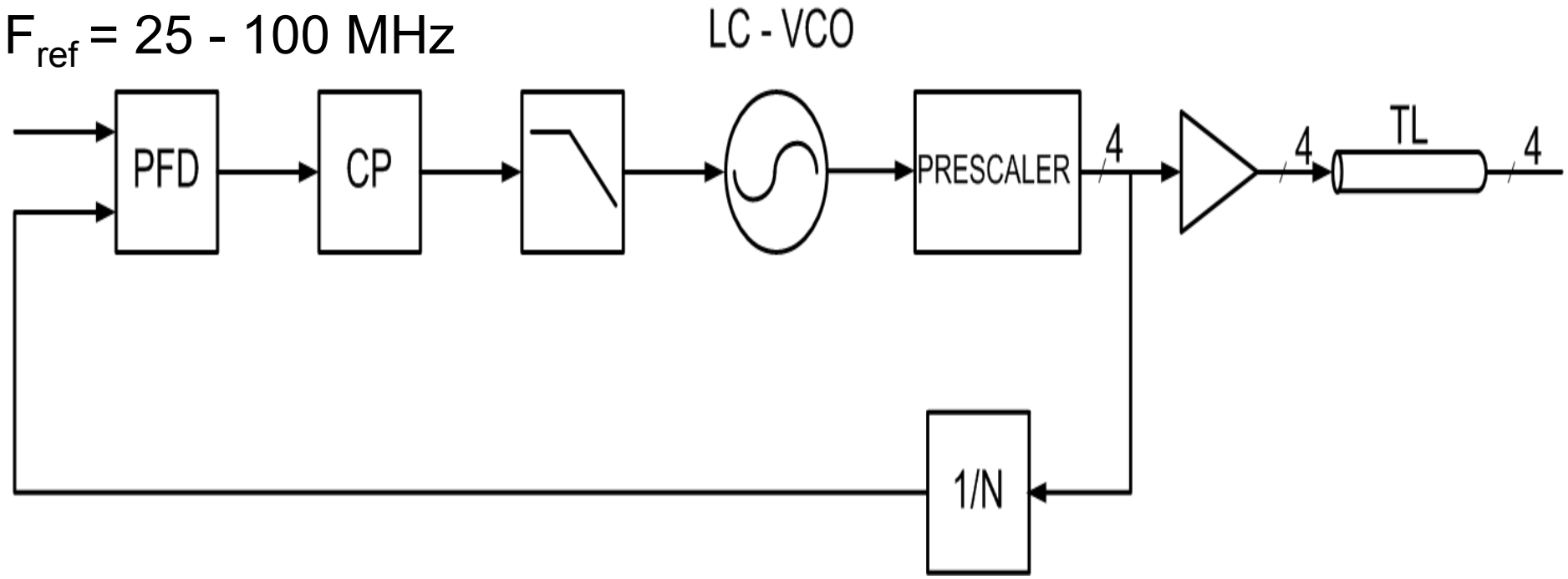
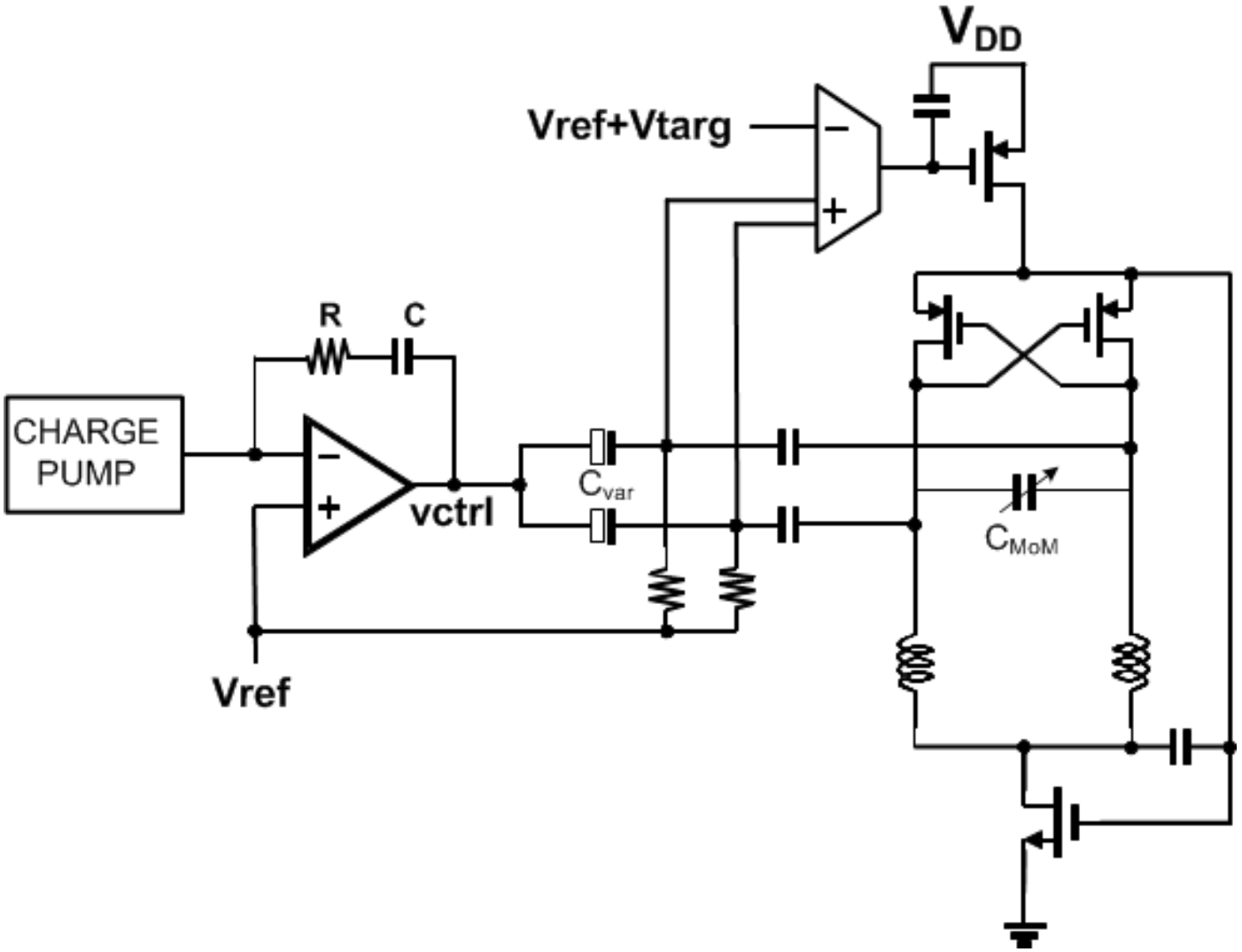
Clock Generation



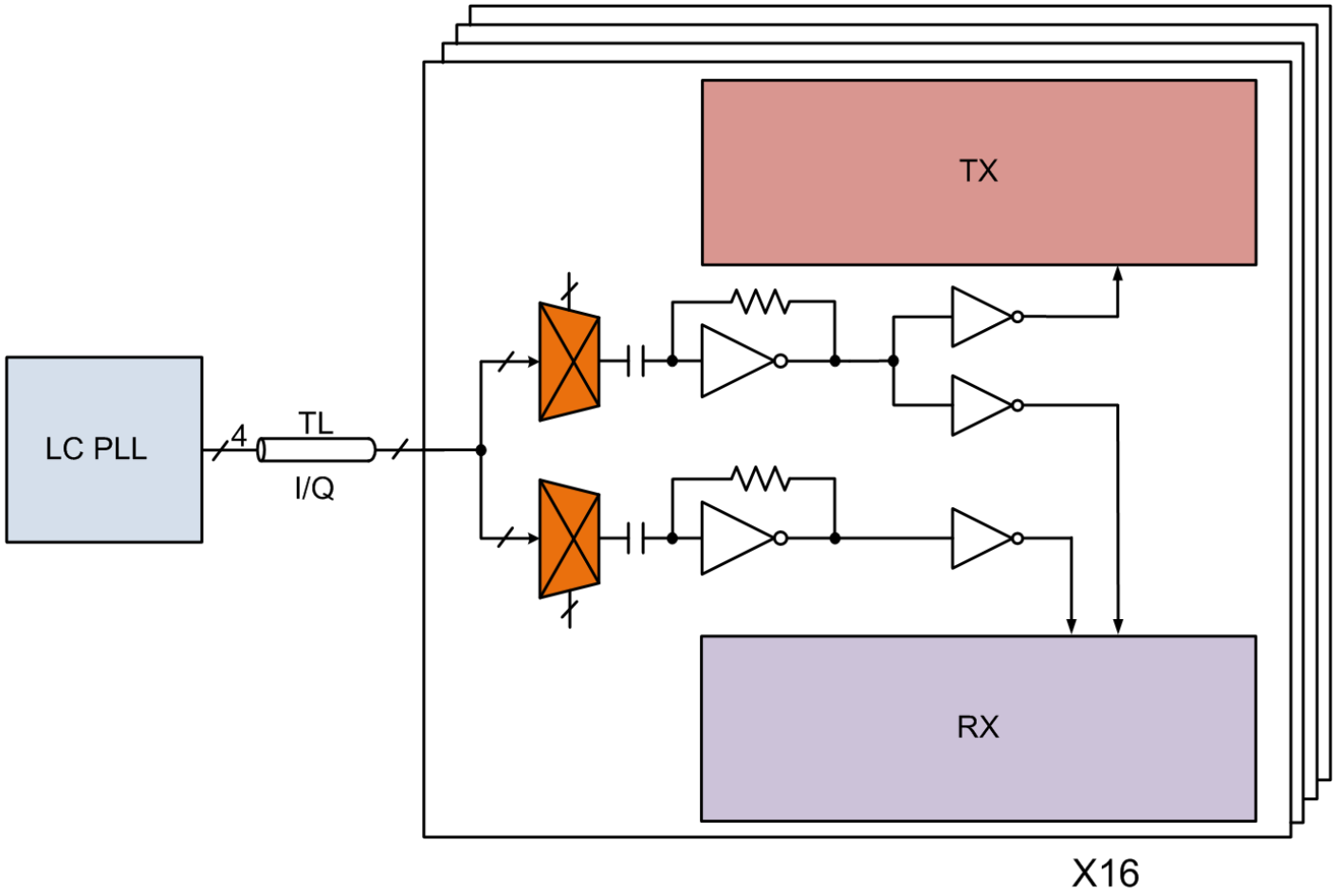
- PLL generates half-rate clocks for IOLANES
- Half-rate clock distribution through transmission line
- Single LC VCO with large tuning range

LPF and VCO



- LC-VCO tuning range is 14 – 22.5 GHz

IOLANE Clocking



- PI resolution is UI/64
- Variable Tx launch phase

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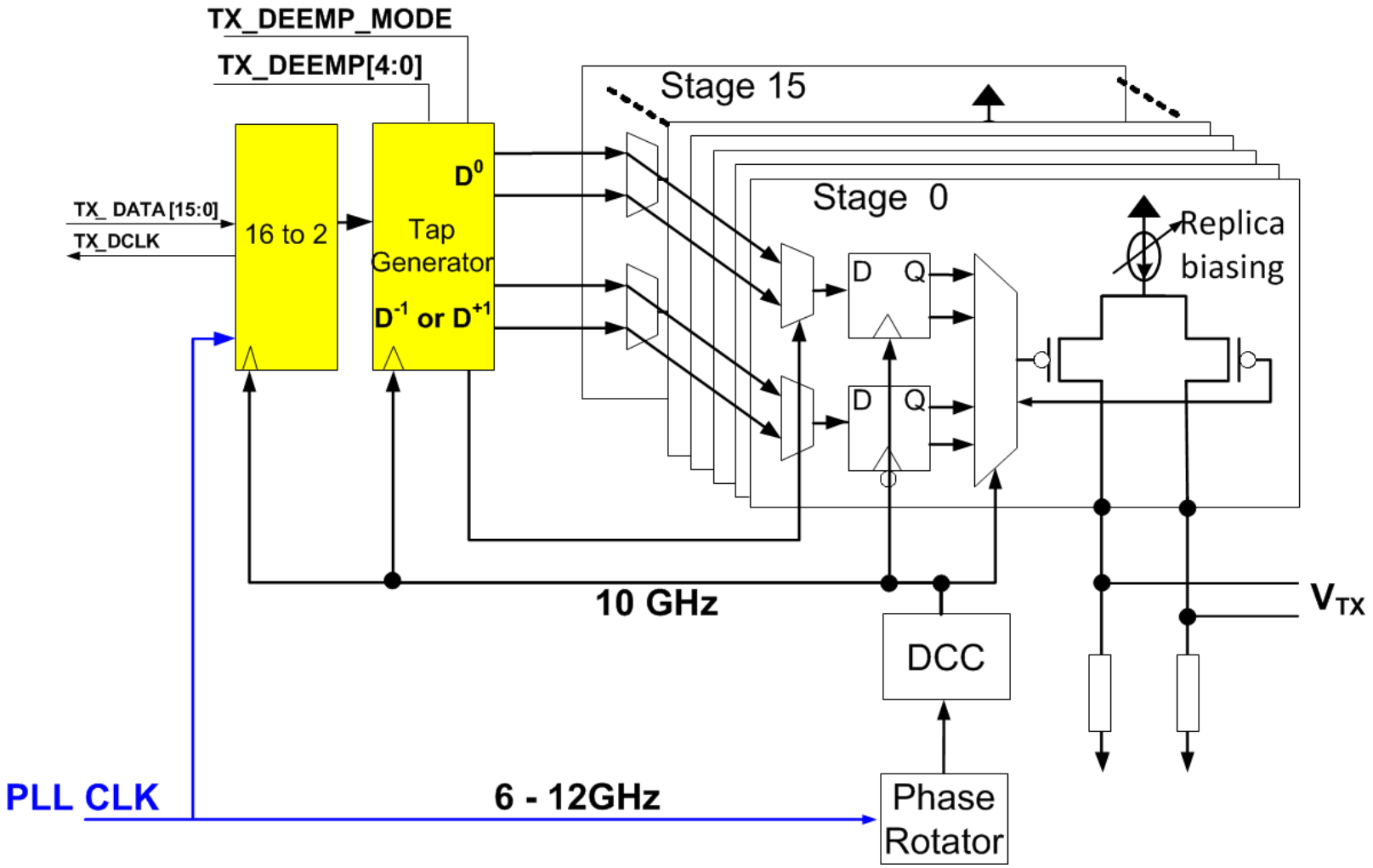
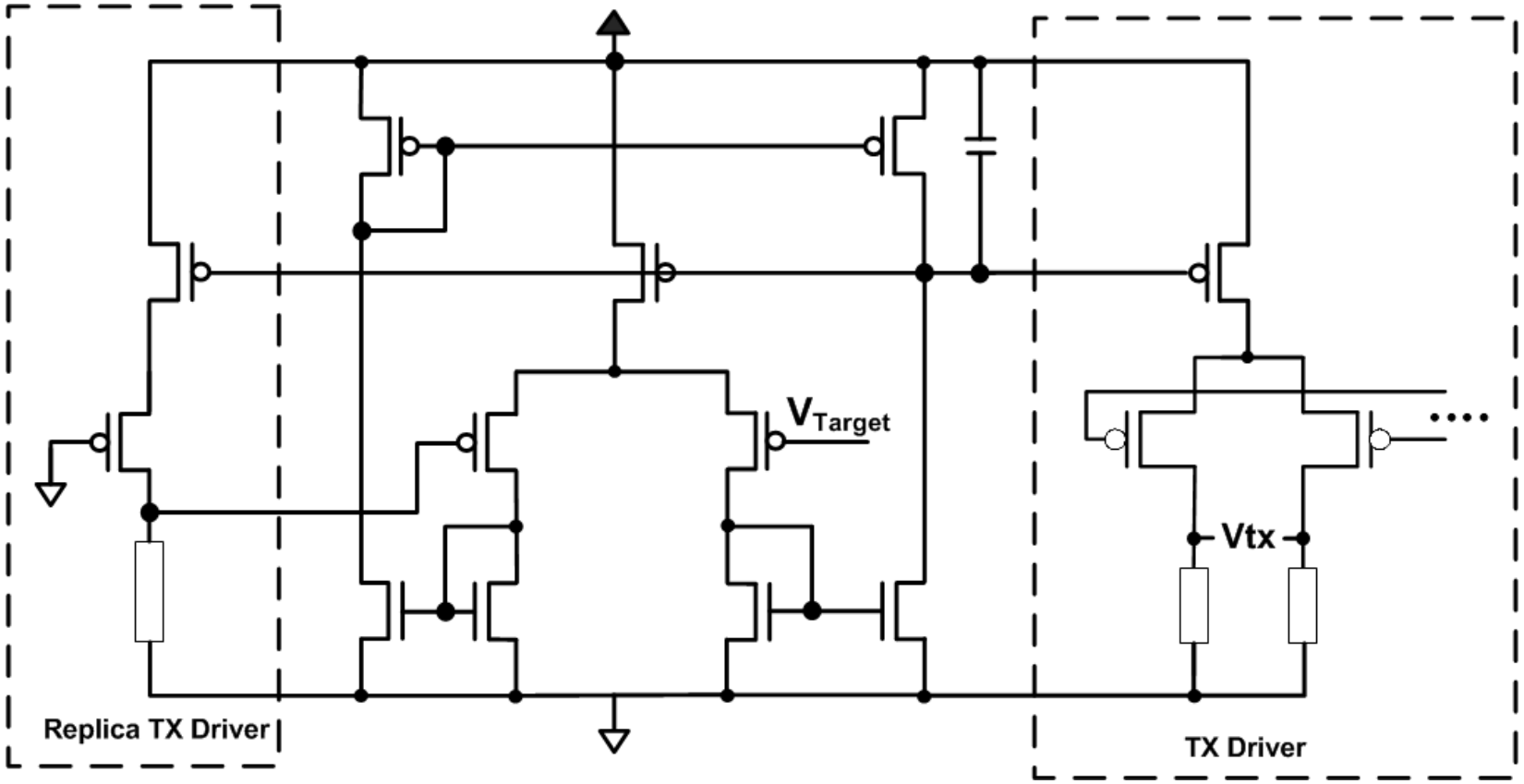
Transmitter Architecture



- 1-tap FFE which can be configured as a pre or post cursor tap
- CML driver for low swing and better power scaling

Replica Biasing of TX Driver



- < 2ns start up time
- Amplitude range = [$0.3V_{ppd}$, $0.6V_{ppd}$]
- Consumes 600uA @ V_{Target} = 500mV

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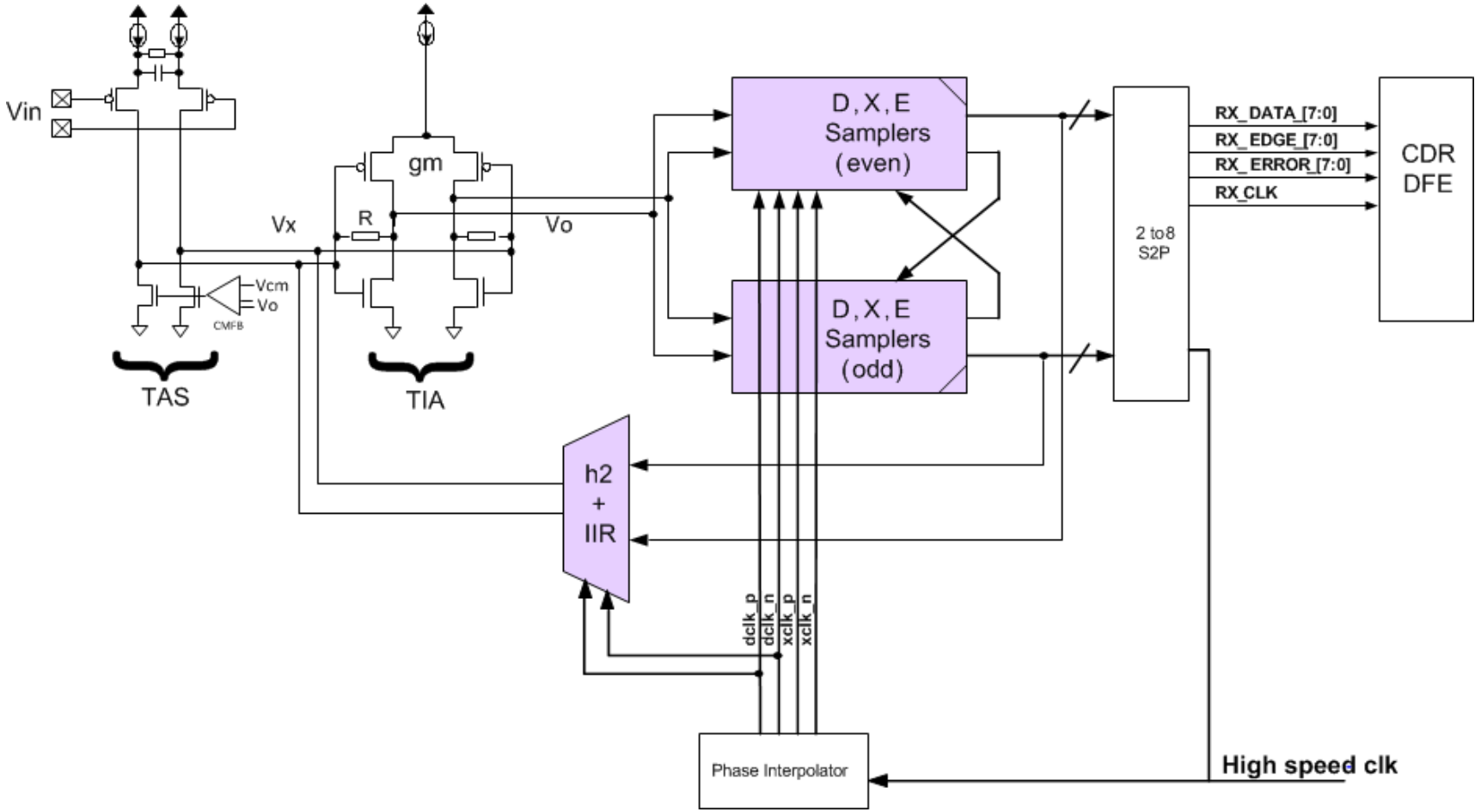
RX Overview



- Single Stage CTLE
- Half-rate 2-tap DFE and Single-Pole IIR
- Direct feedback of H_1, H_2 and H_X taps.

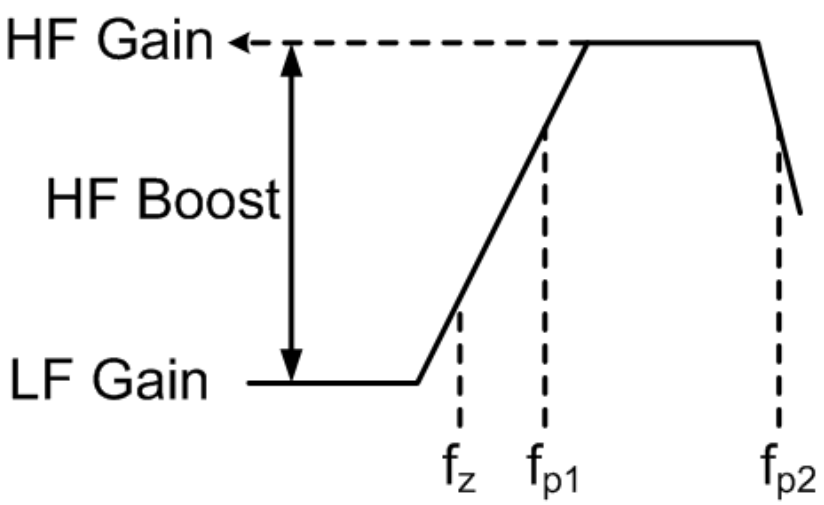
Conventional CTLE + DFE

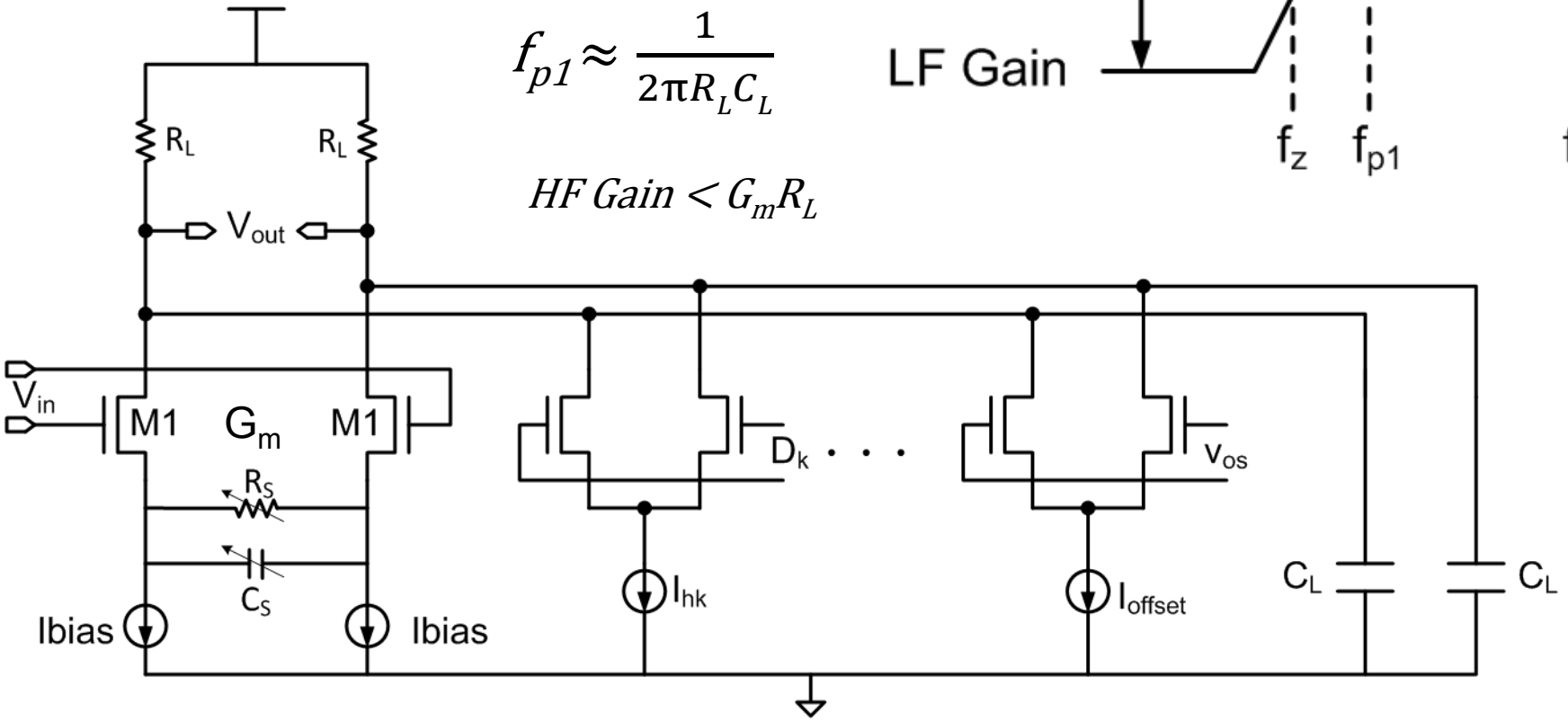
$$f_z \approx \frac{1}{2\pi R_s C_s}$$

$$f_{p2} \approx \frac{1+G_m R_s}{2\pi C_s}$$

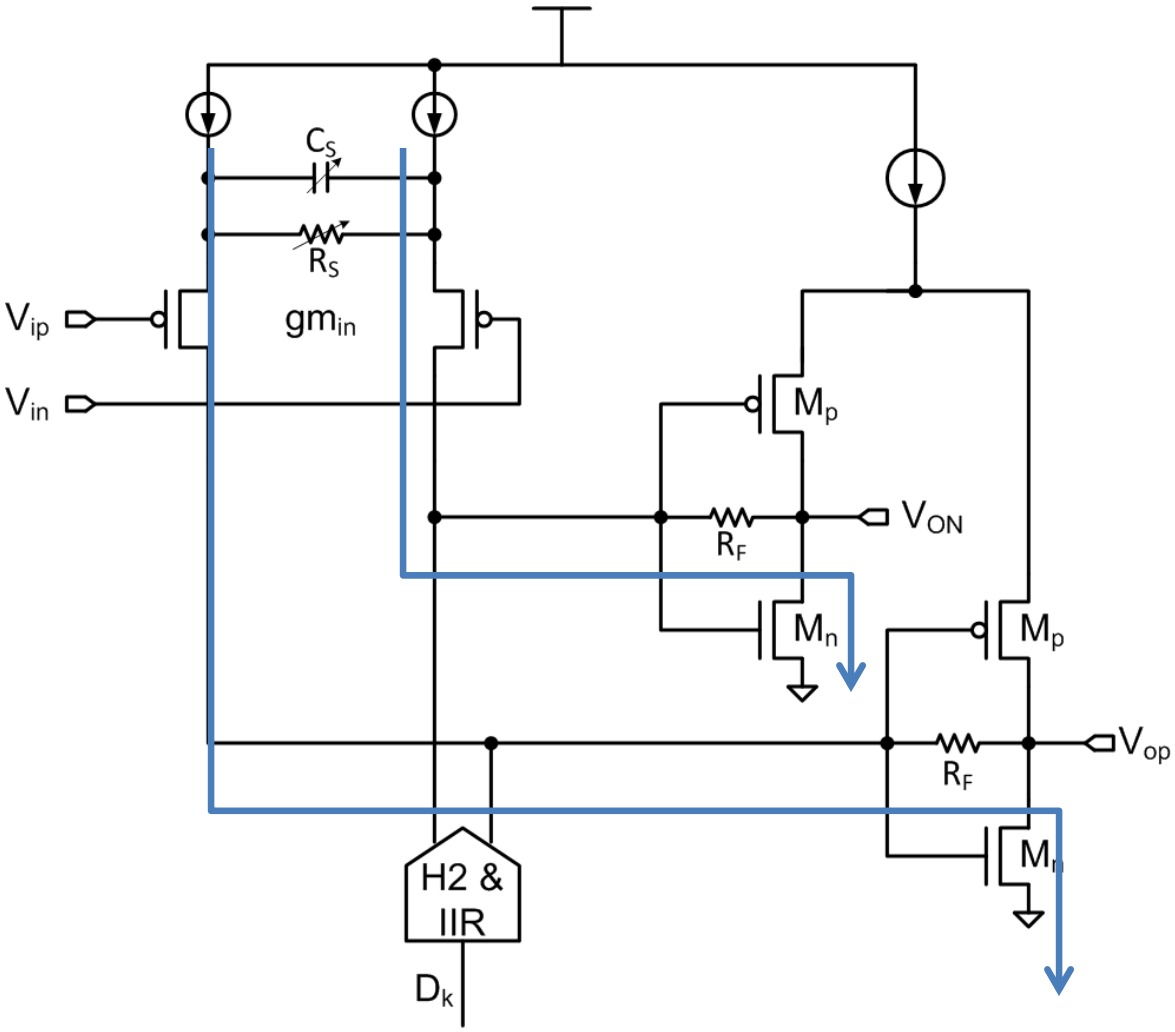
$$f_{p1} \approx \frac{1}{2\pi R_L C_L}$$

$$HF\ Gain < G_m R_L$$





Proposed CTLE + DFE



TAS :

$$\omega_z \approx \frac{1}{R_s C_s}$$

$$\omega_p \approx \frac{1+Gm_{in}Rs}{C_s}$$

TIA:

$$A = (Gm_p + Gm_n)(Rds_p // Rds_n)$$

$$R_{TIA} = \frac{A}{1+A} R_F$$

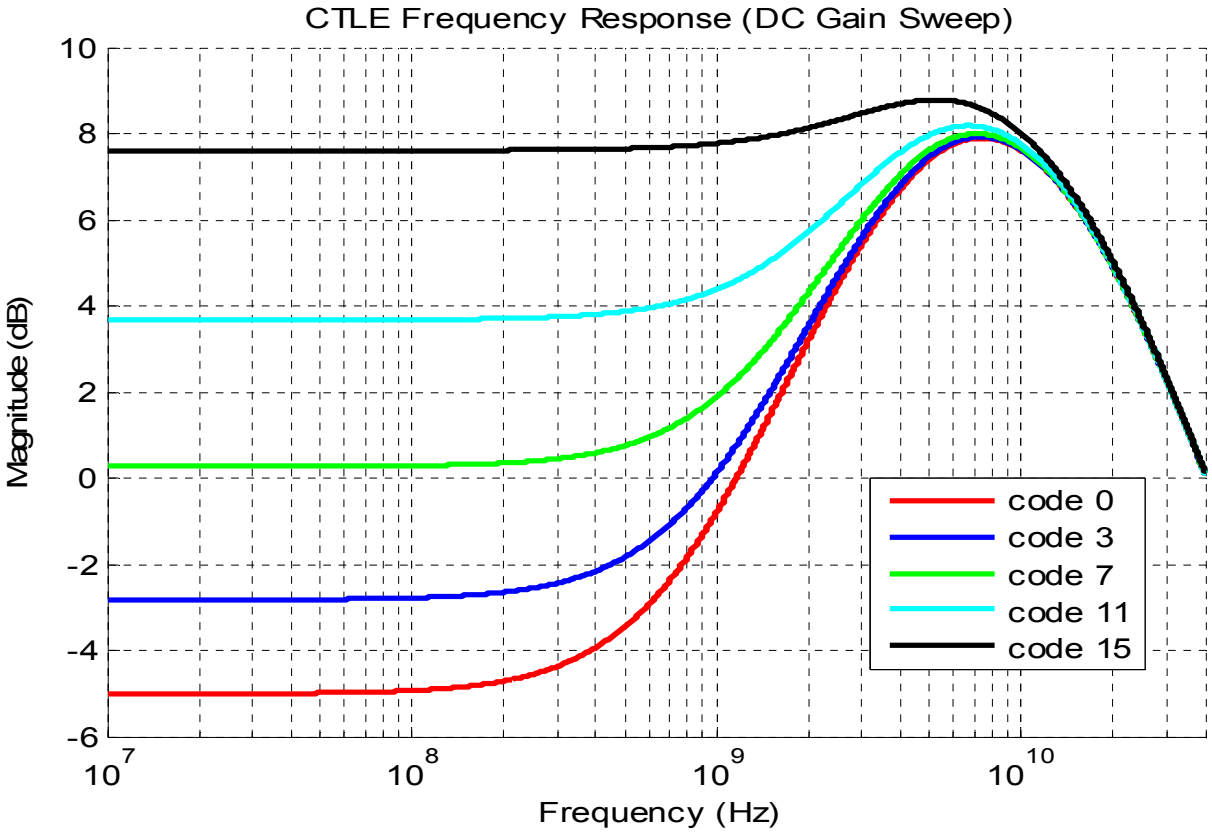
$$R_{in} = \frac{1}{1+A} R_F$$

$$R_{out} \approx \frac{1}{(Gmp + Gmn)}$$

- Low impedance at TIA input and output
- I_{h2} & I_{IIR} is quite small since R_{TIA} is ~R_f

$$HF\ Gain \sim Gm_{in}R_F$$

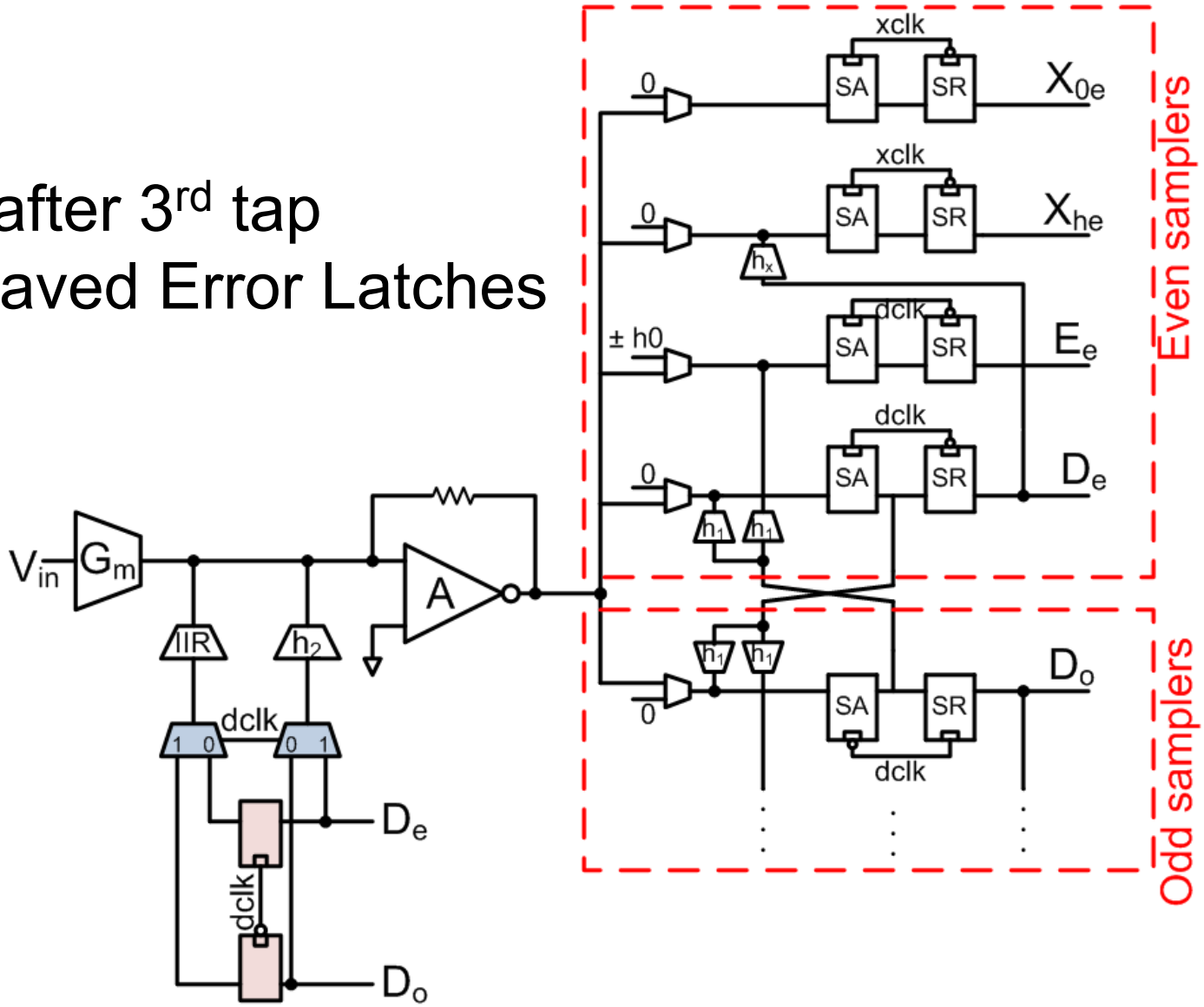
Simulated CTLE Response



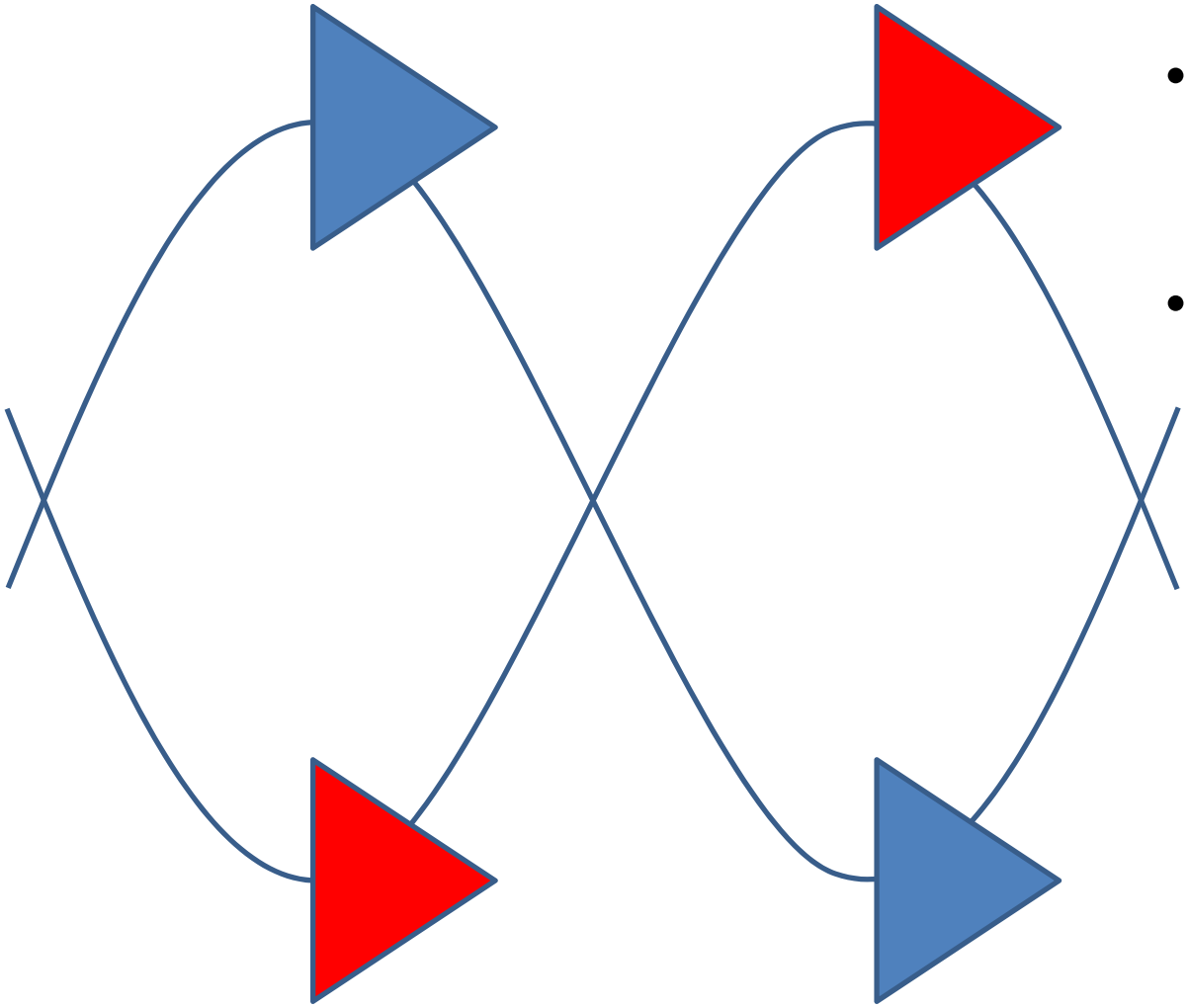
- Worst case HF gain of 8dB
- Gain peaking at 8.5GHz

DFE & IIR Architecture

- Direct DFE
- Edge DFE
- IIR applied after 3rd tap
- Time interleaved Error Latches

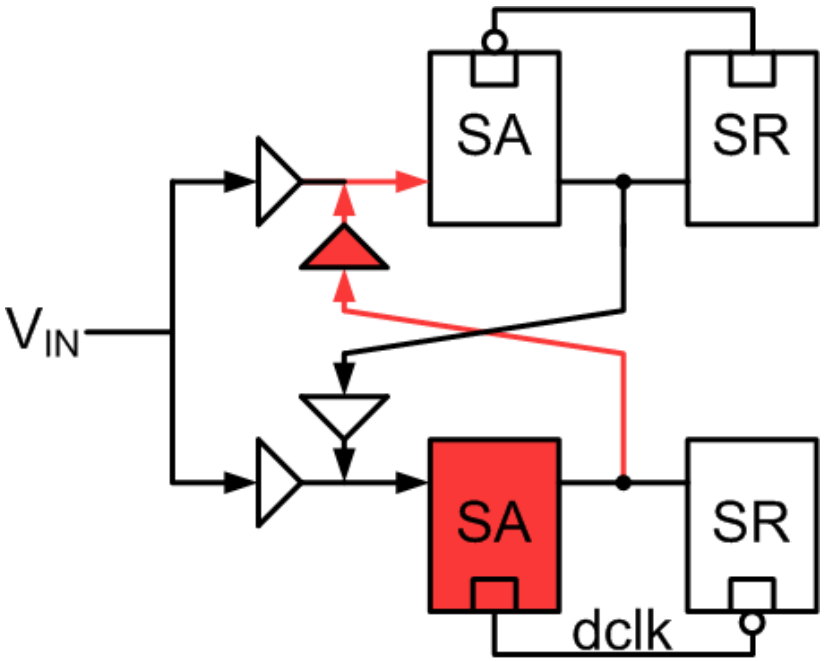


Error Samplers



- Time interleaved error generation
- 50% savings in Power and Area

H_1 timing

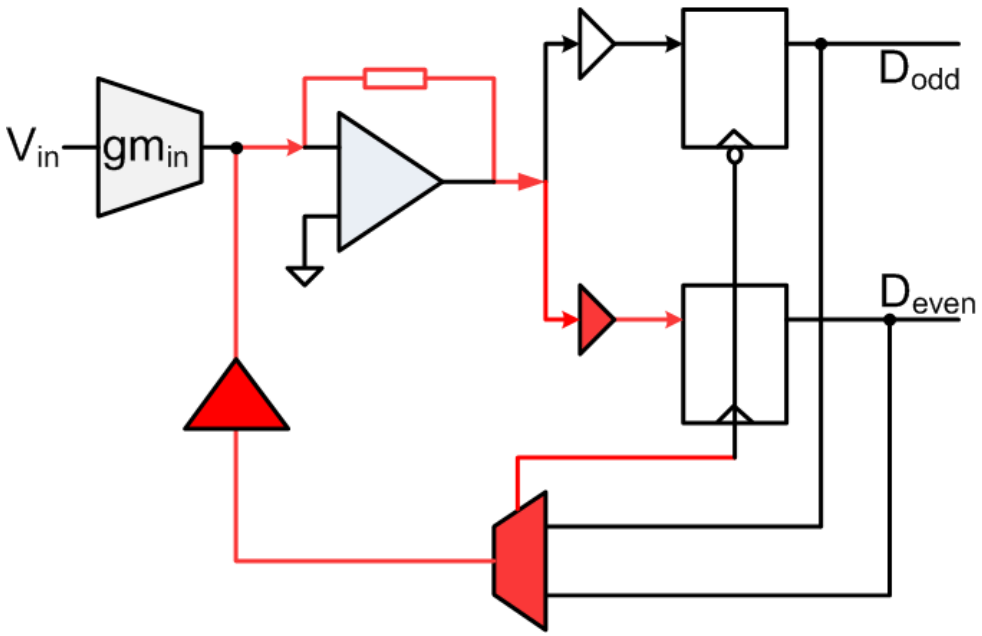


H_1 Timing Constraint:

$T_{Clk\text{-}q} + T_{Prop} + T_{Setup} < 1UI$

Simulated Worst case Margin @ 20Gbps = 10ps

H_2 timing

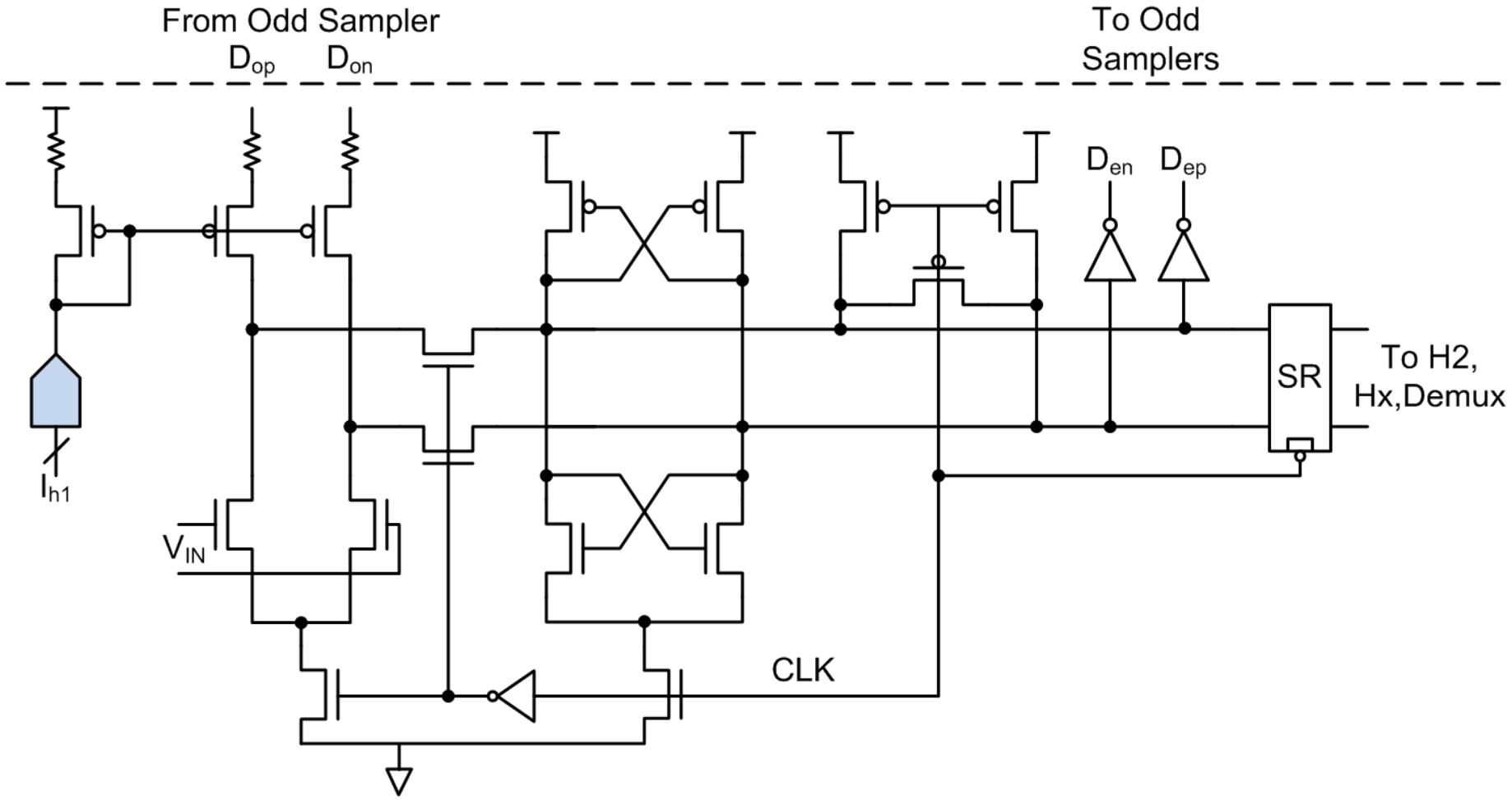


H_2 Timing Constraint:

$T_{Mux} + T_{Tia} + T_{Setup} < 1UI$

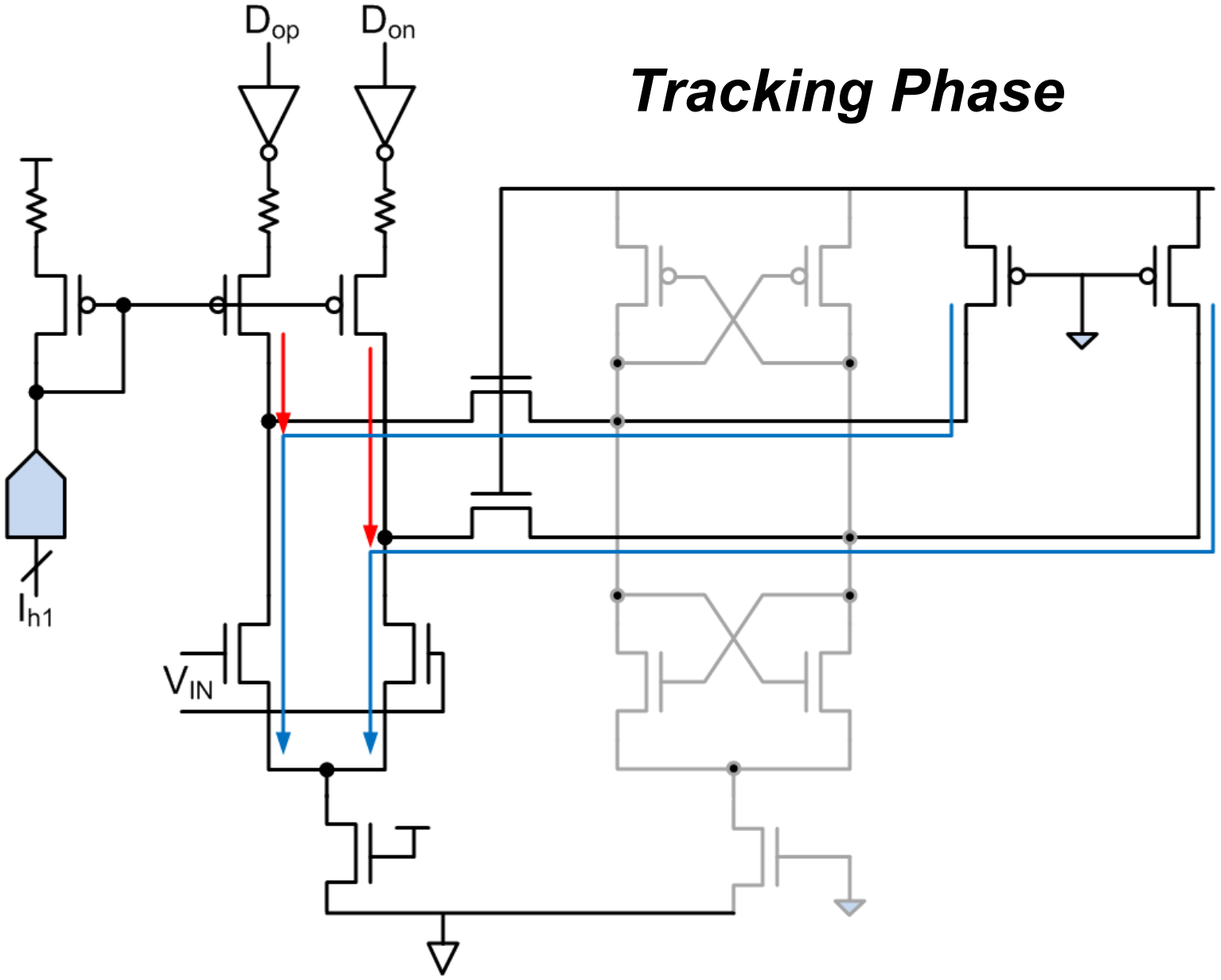
Simulated worst case margin @ 20Gbps = 5ps

CMOS Sampler



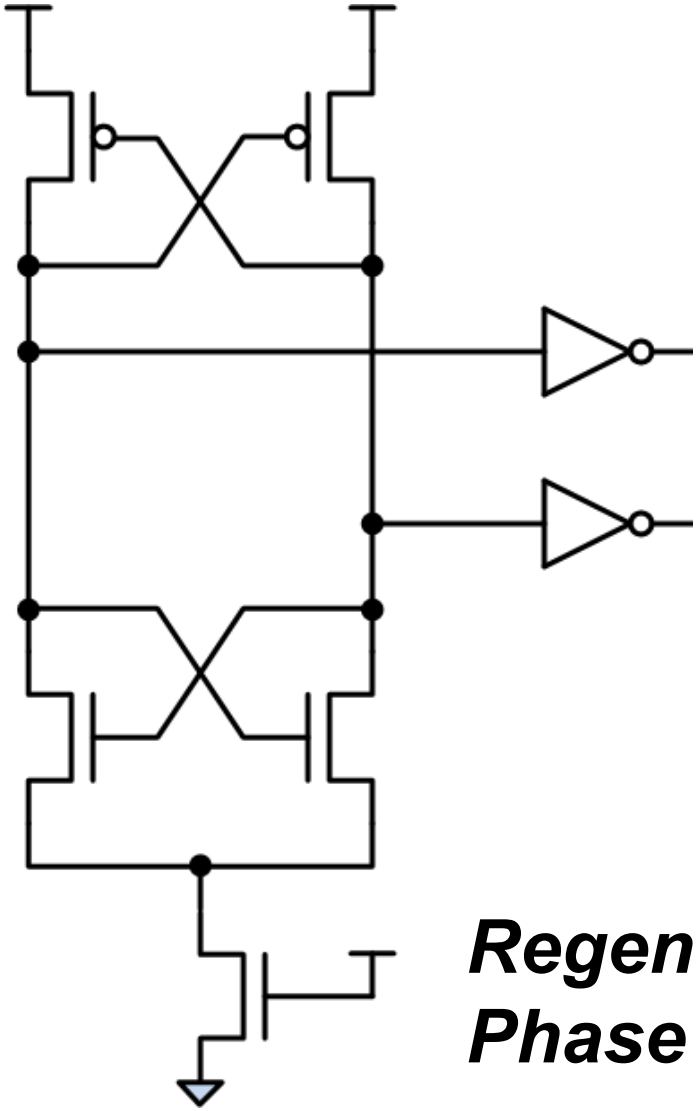
- Worst case sensitivity is < 2mV
- Worst case SA regeneration time-constant, $\tau < 6$ps

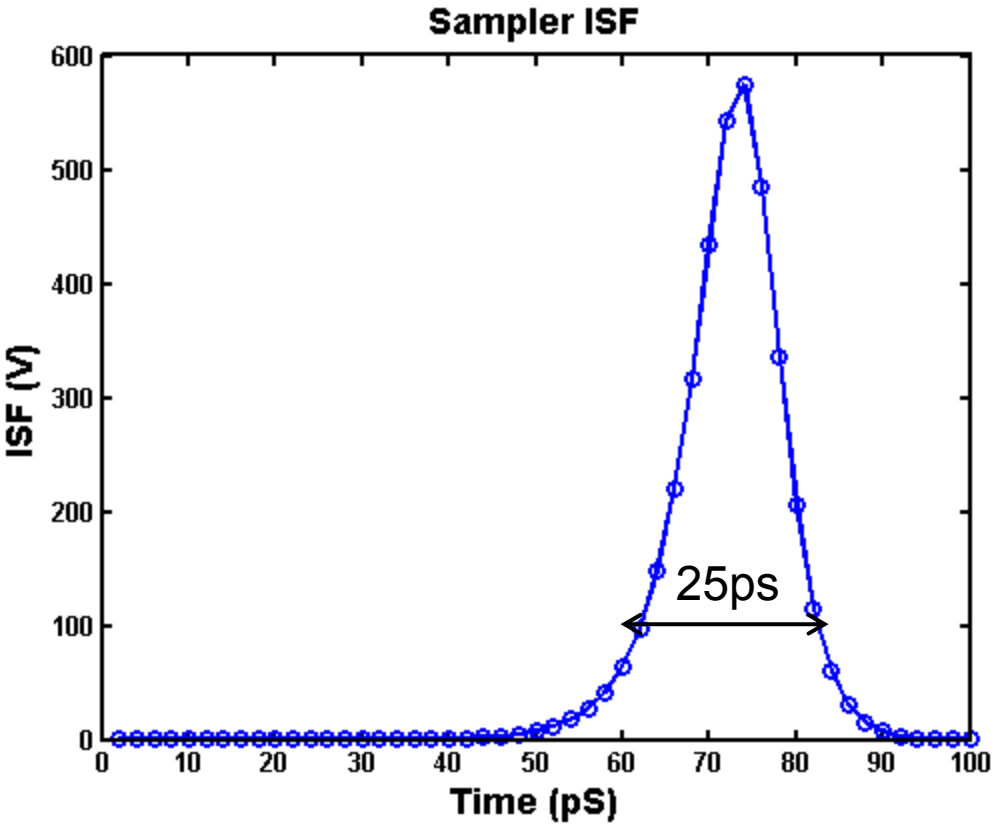
Latch Operation



Tracking Phase

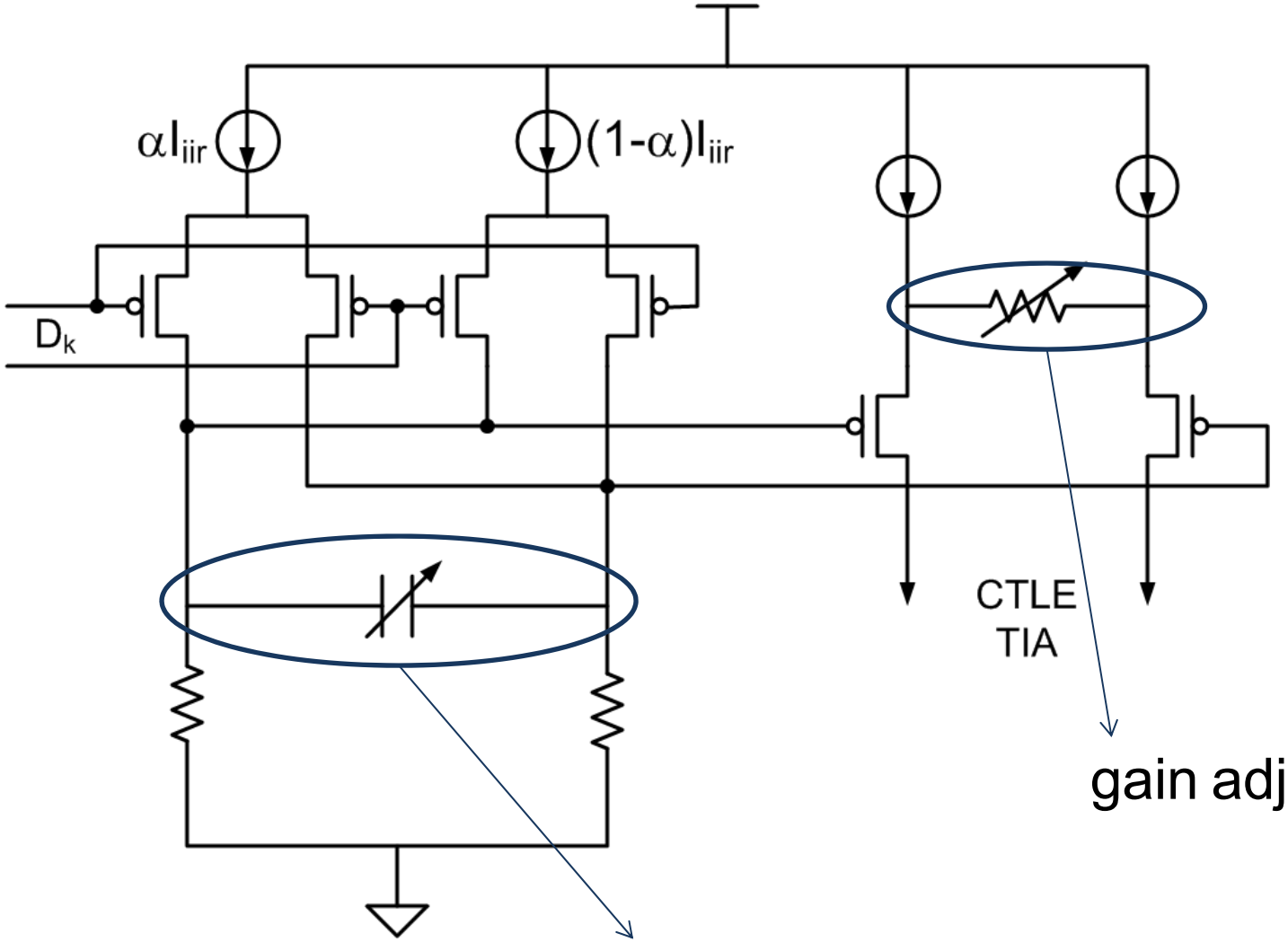
Latch Regeneration





Regeneration Phase

Single–Pole IIR

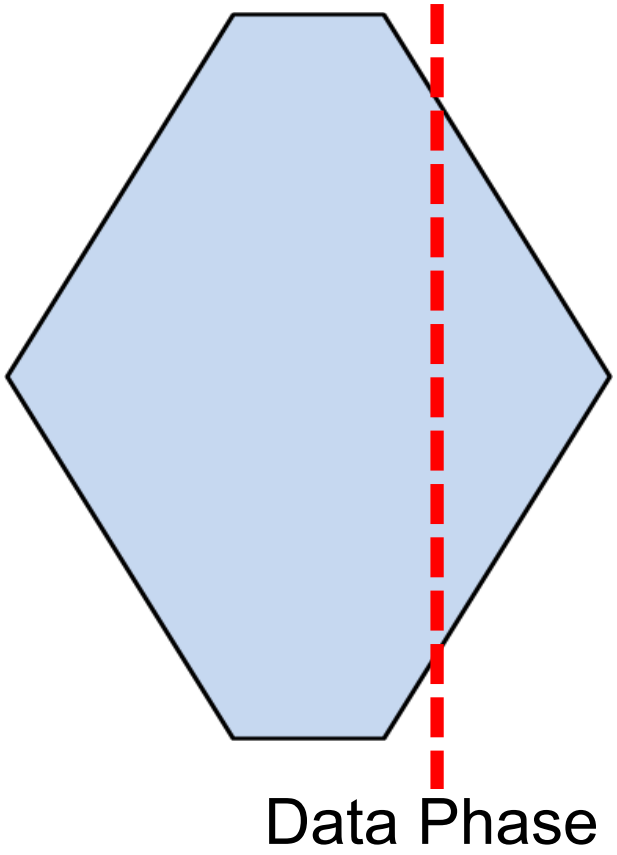


τ = [30ps , 80ps]

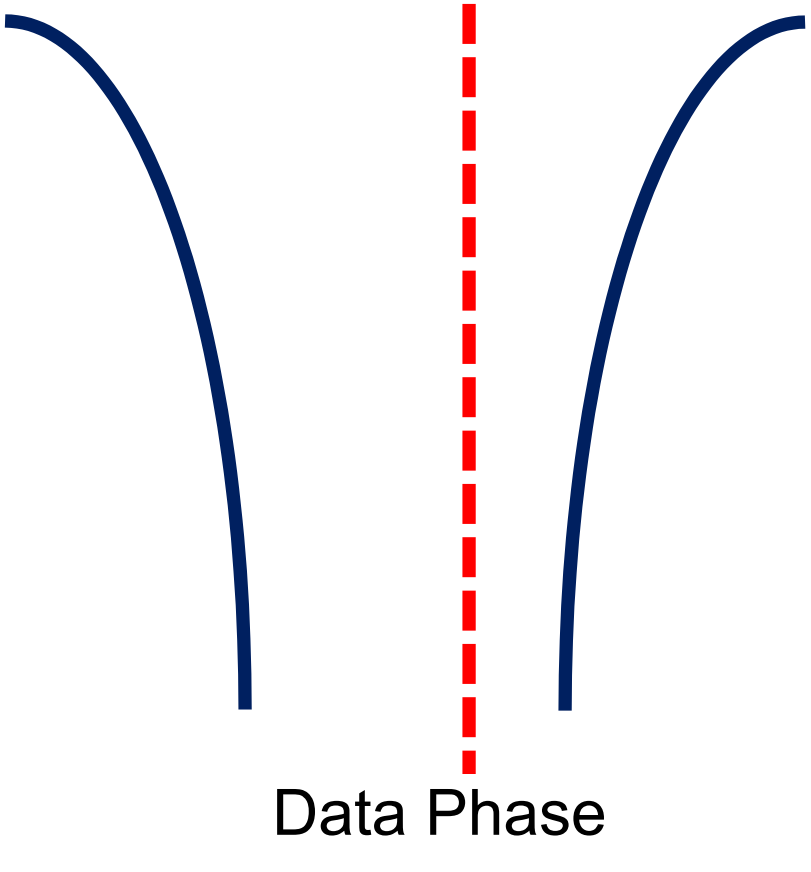
α = 0,1

Edge ISI

Equalized Eye Diagram

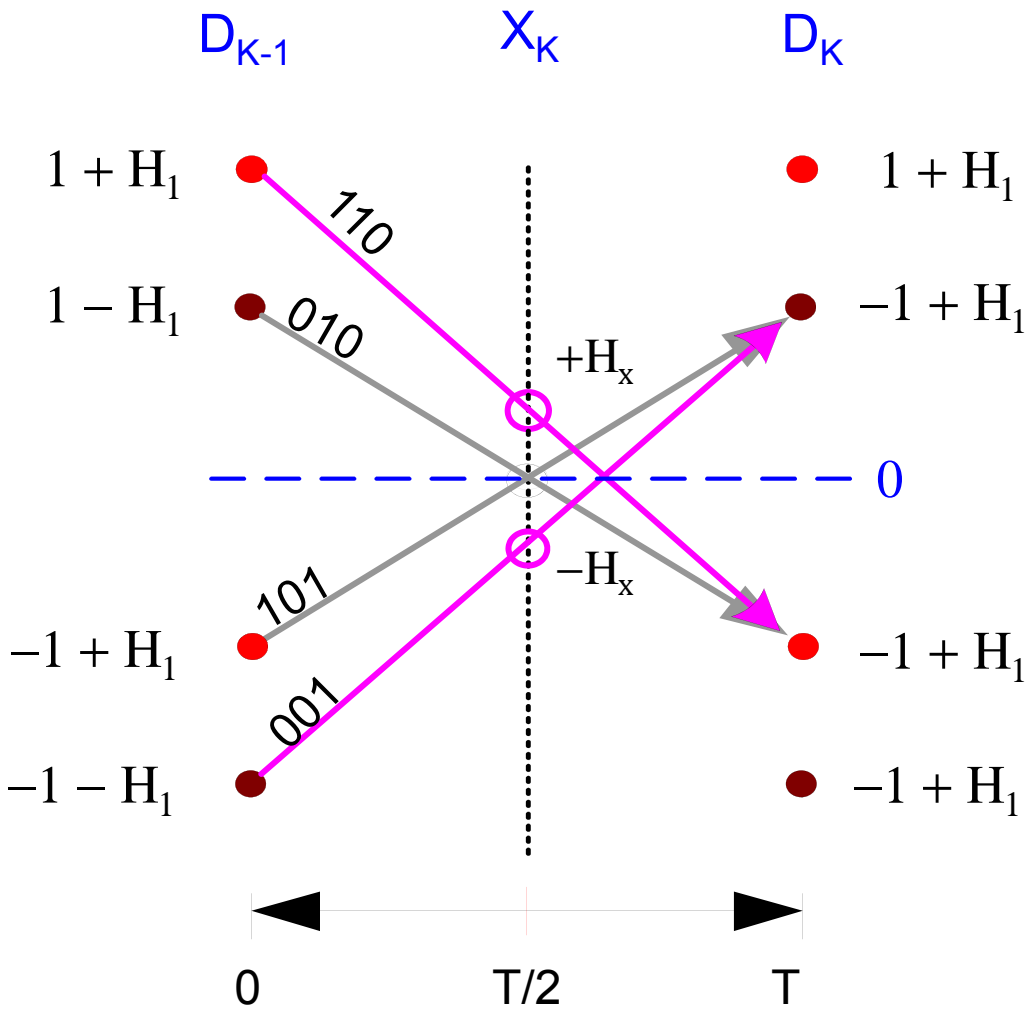


BER Bathtub Curve



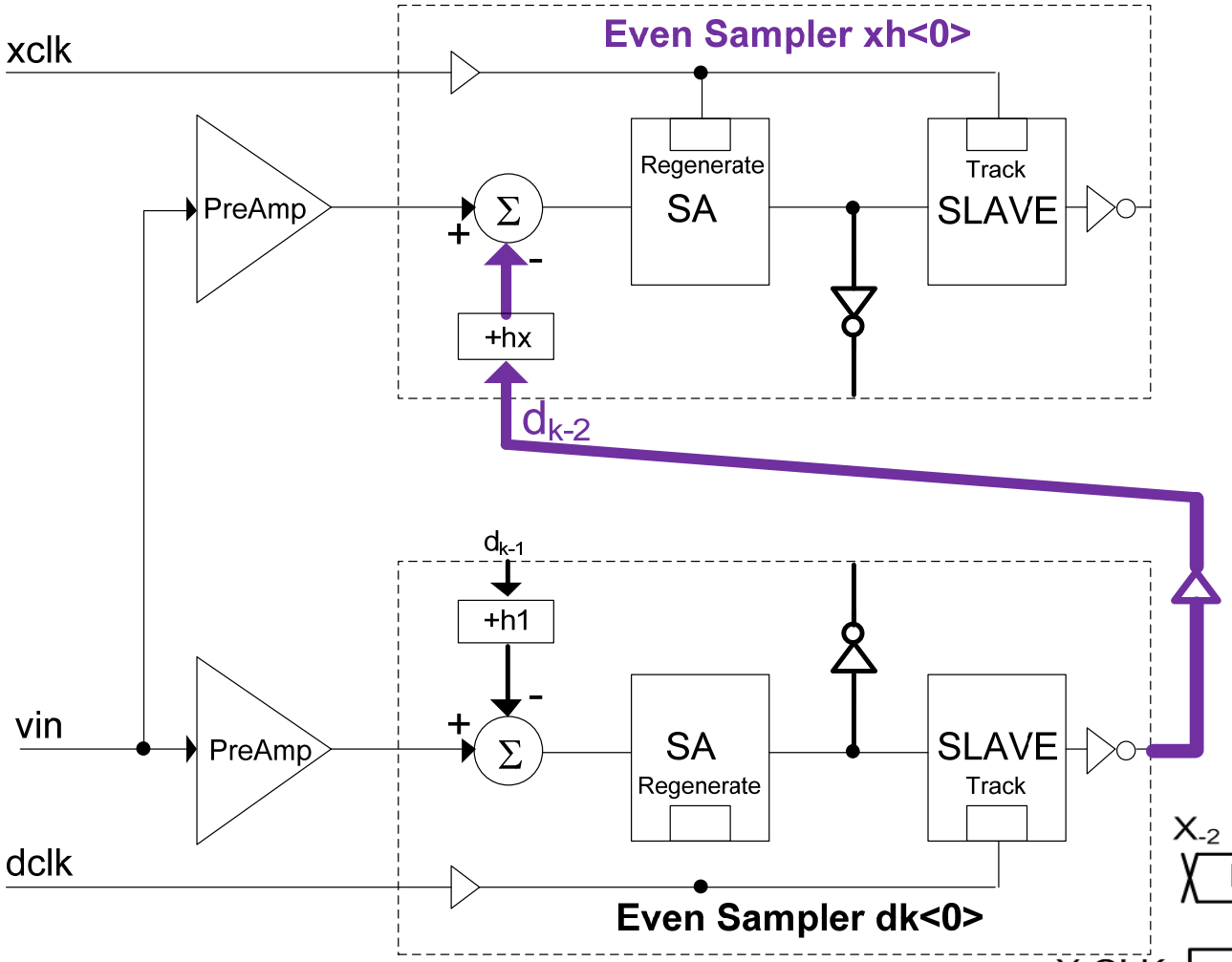
- Suboptimal Data Sampling Phase due to ISI

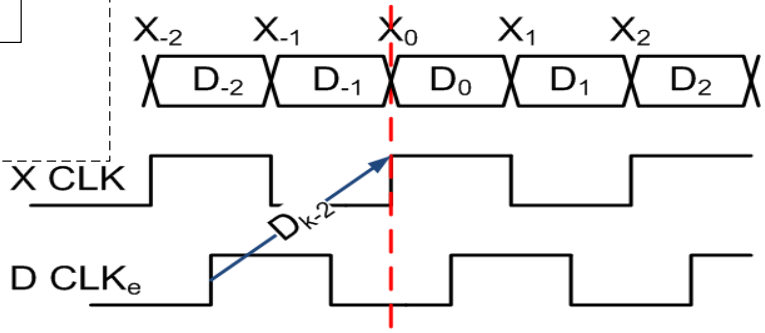
Edge DFE, H_X



d_{k-2}	d_{k-1}	d_k	Edge Type
0	0	1	X_h
0	1	0	X_0
1	0	1	X_0
1	1	0	X_h

Edge DFE Implementation





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Receiver Adaptation

Loop	Gradient	Comments
H0	$e_k.d_k$	Cursor tap
H1	$e_k.d_{k-1}$	First DFE tap
H2	$e_k.d_{k-2}$	Second DFE tap
Hx or IQ offset	$e_k.d_{k+1}$	Edge DFE
IIR Gain	$e_k \cdot sgn(d_{k-3} + d_{k-4} + d_{k-5} + d_{k-6})$	IIR gain adjustment
IIR Pole	$e_k \cdot sgn(d_{k-3} - d_{k-4})$	Adjust tail of IIR response Fixed after Initial training
CTLE_C (HF gain)	$e_k \cdot sgn(d_{k-1} - d_{k-3})$	Adjust HF gain Fixed after initial training
CTLE_R (LF gain)	$e_k \cdot sgn(d_{k-1} + d_{k-2})$	Adjust LF gain Fixed after initial training
CDR	$x_k.d_{k-1}$	Bang-Bang CDR

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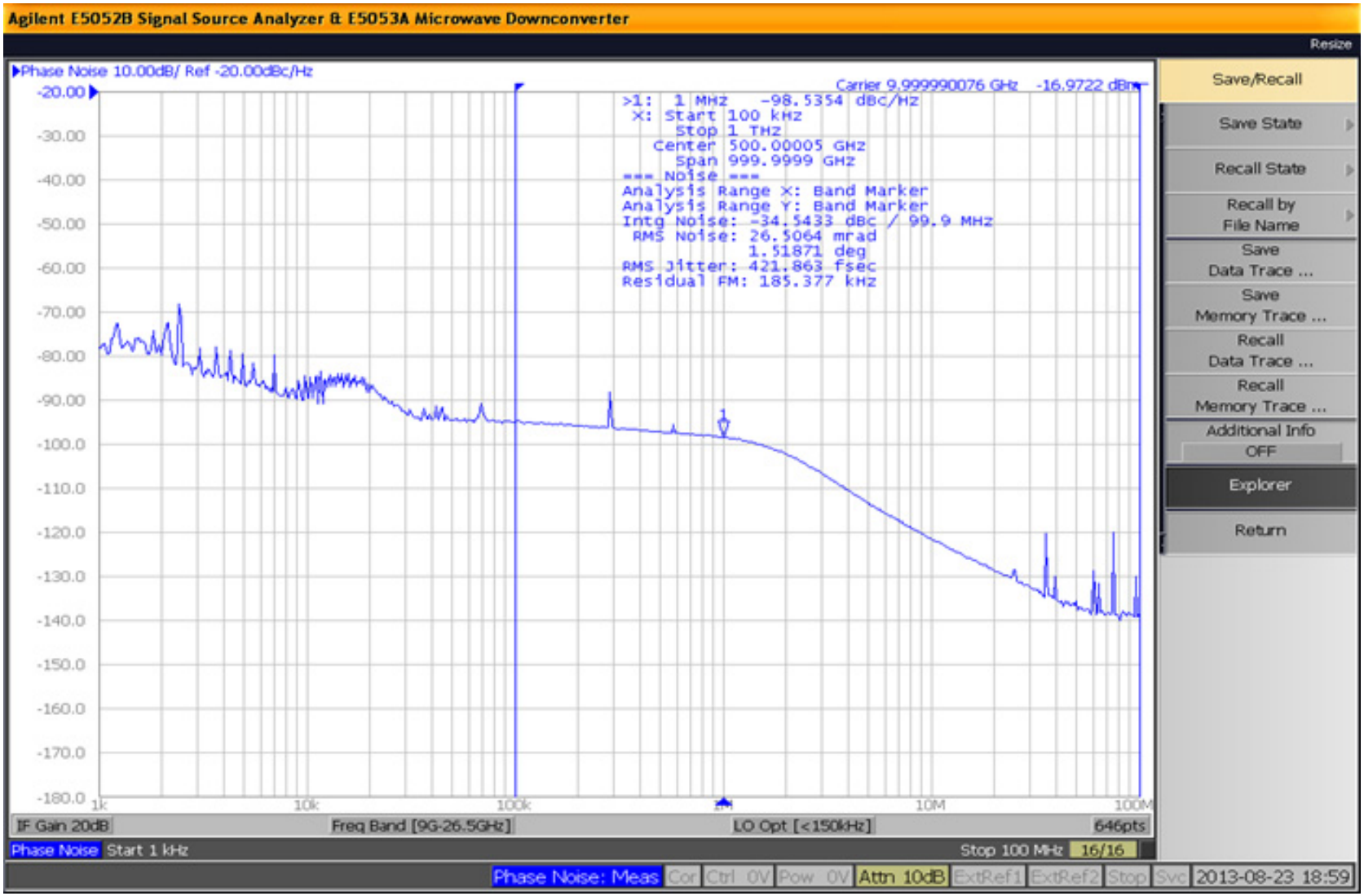
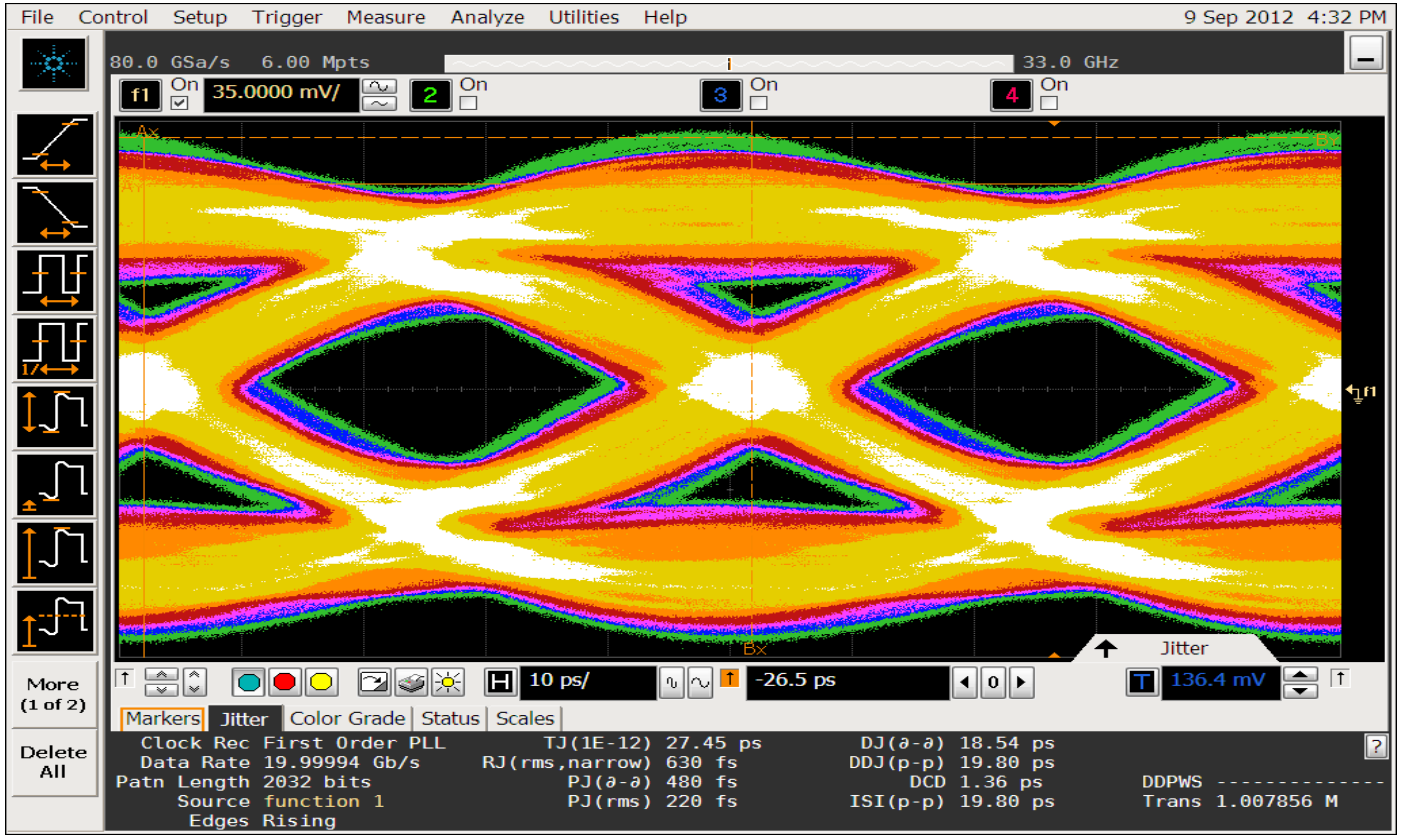
PLL Performance



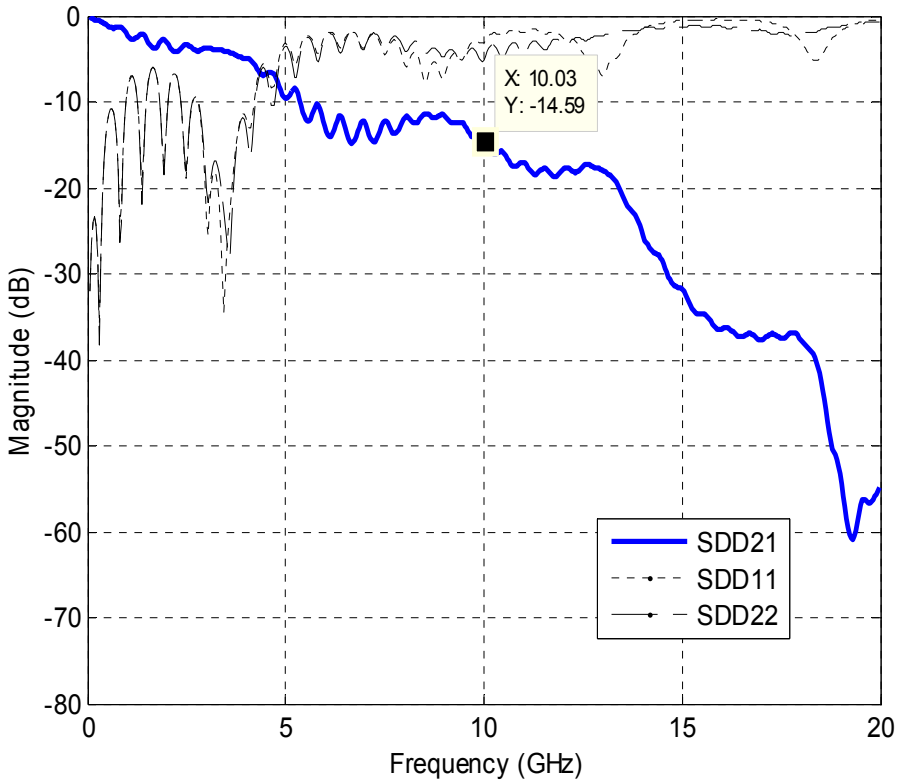
- Phase Noise at TX with 20Gbps Nyquist pattern

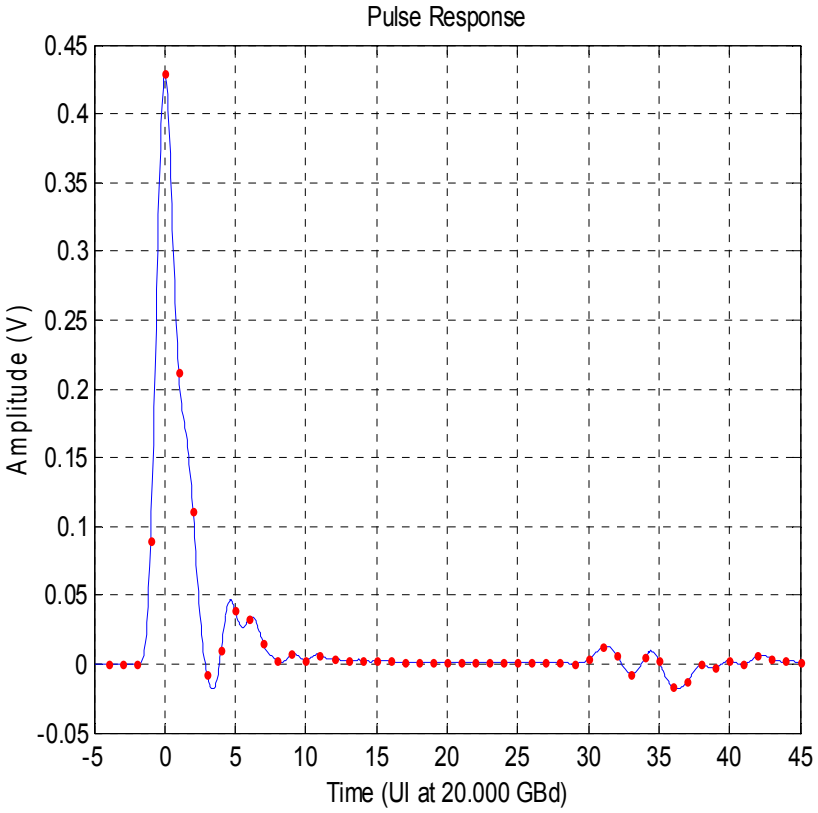
Measured TX Result



- 20Gb/s TX eye diagram with 9dB of Pre-Emphasis

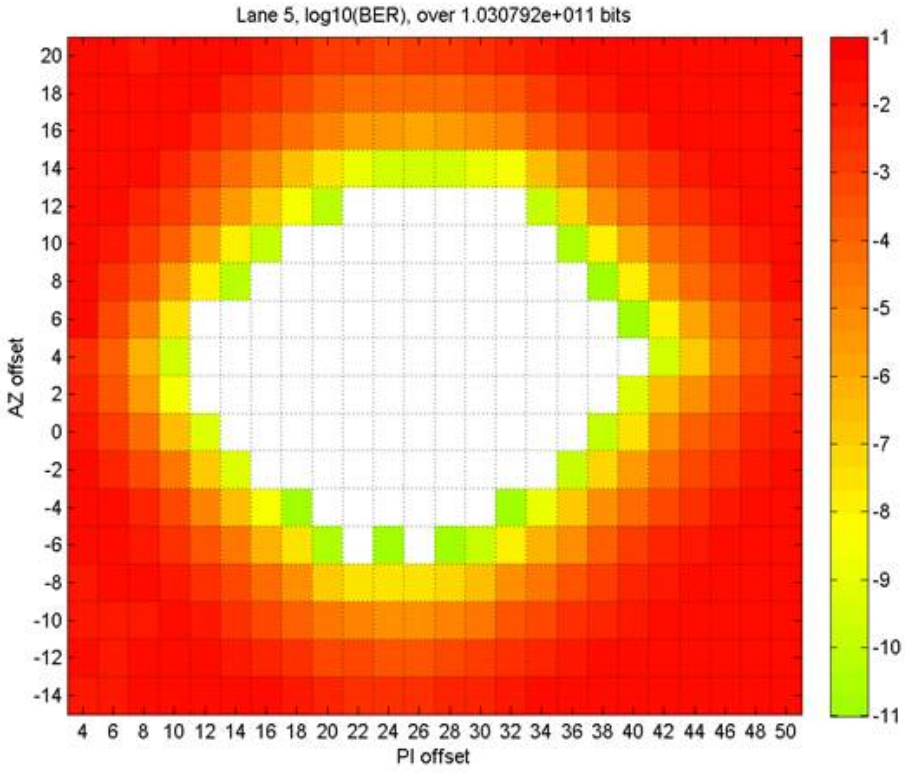
Test Channel Characteristics

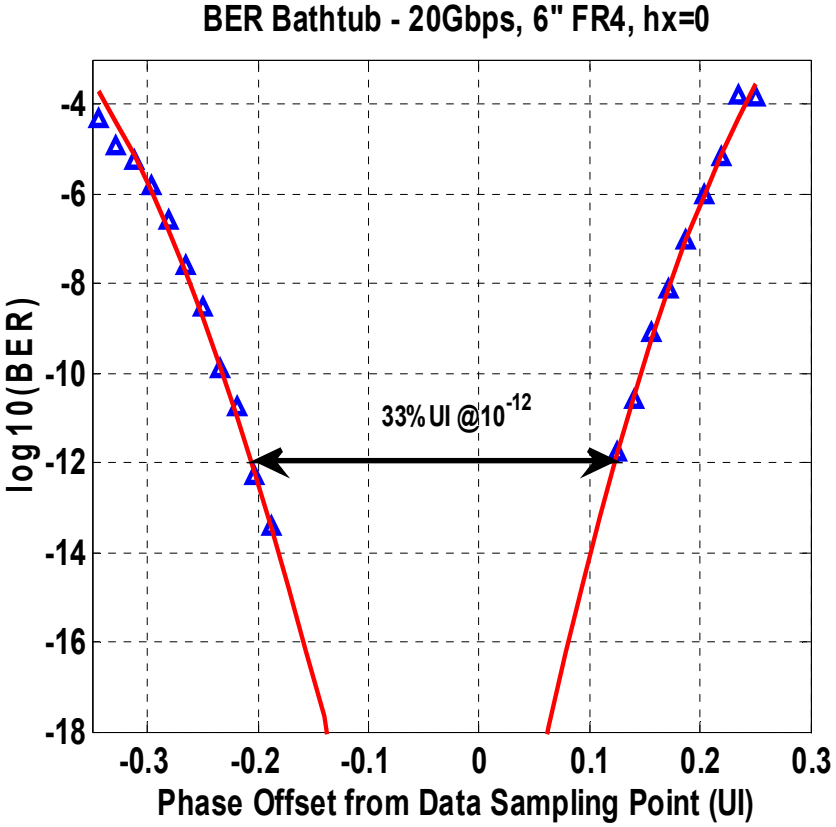




- Response of test channel and unequalized pulse response

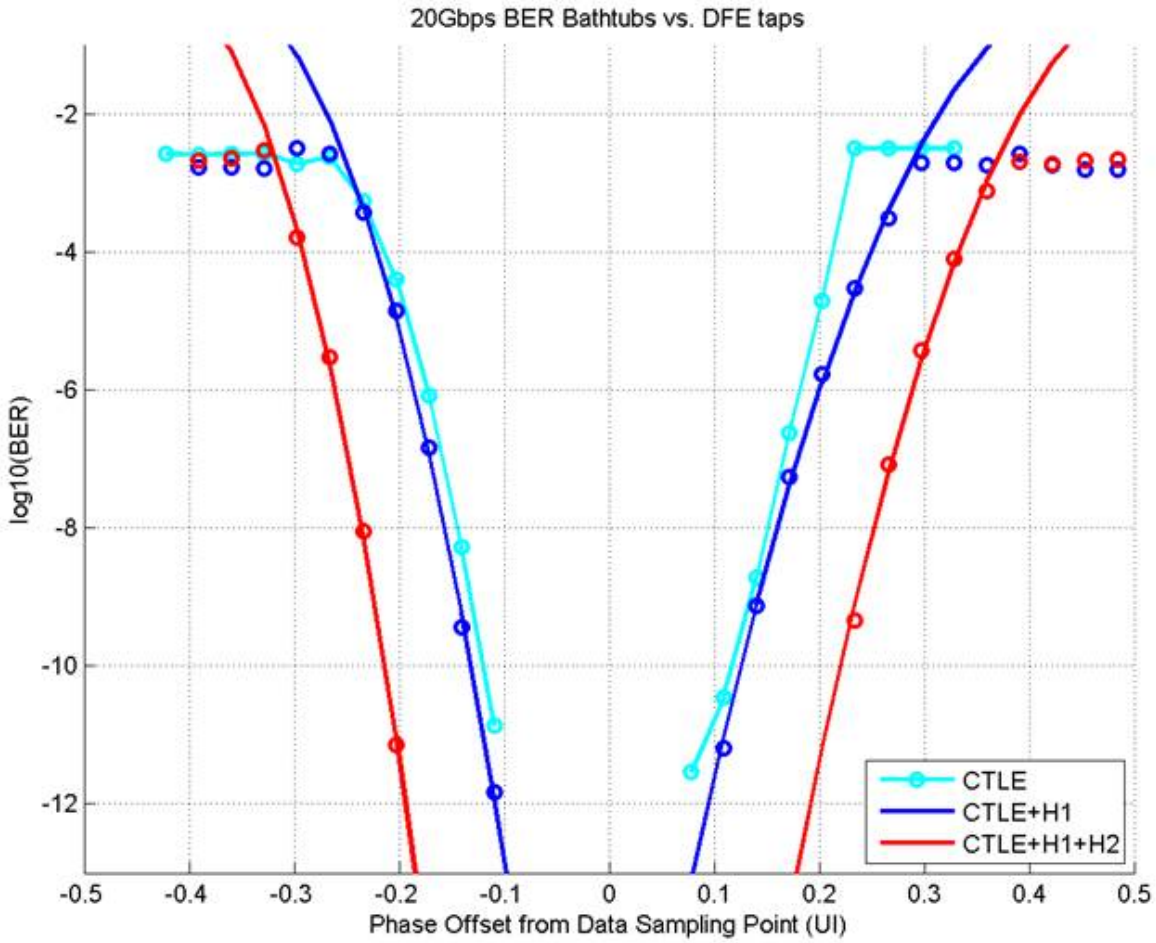
Equalized RX Eye diagram at 20Gbps





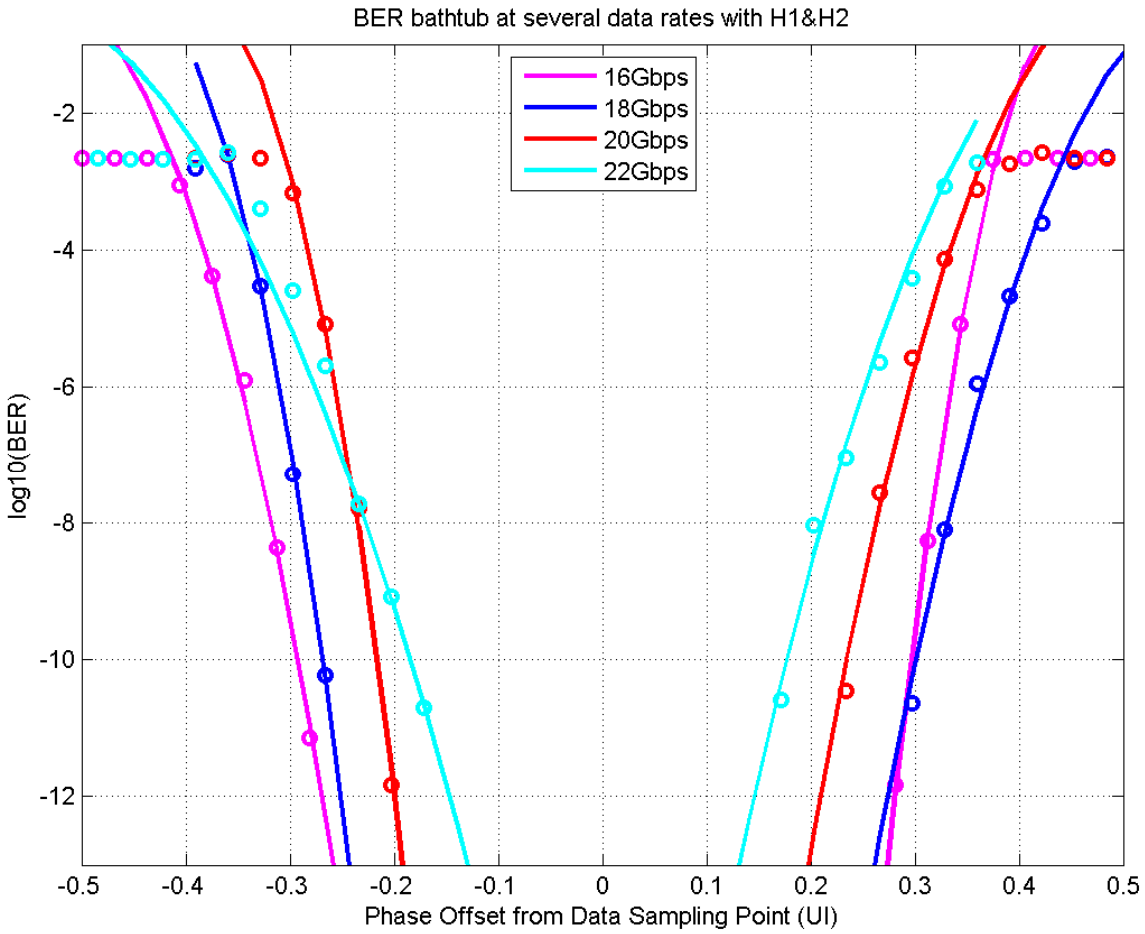
- ± 60mV of vertical opening @ 10^{-12} with PRBS31 pattern
- 0.2UI horizontal eye opening at 10^{-18} BER without IQ offset adaptation

Equalized RX bathtub curves



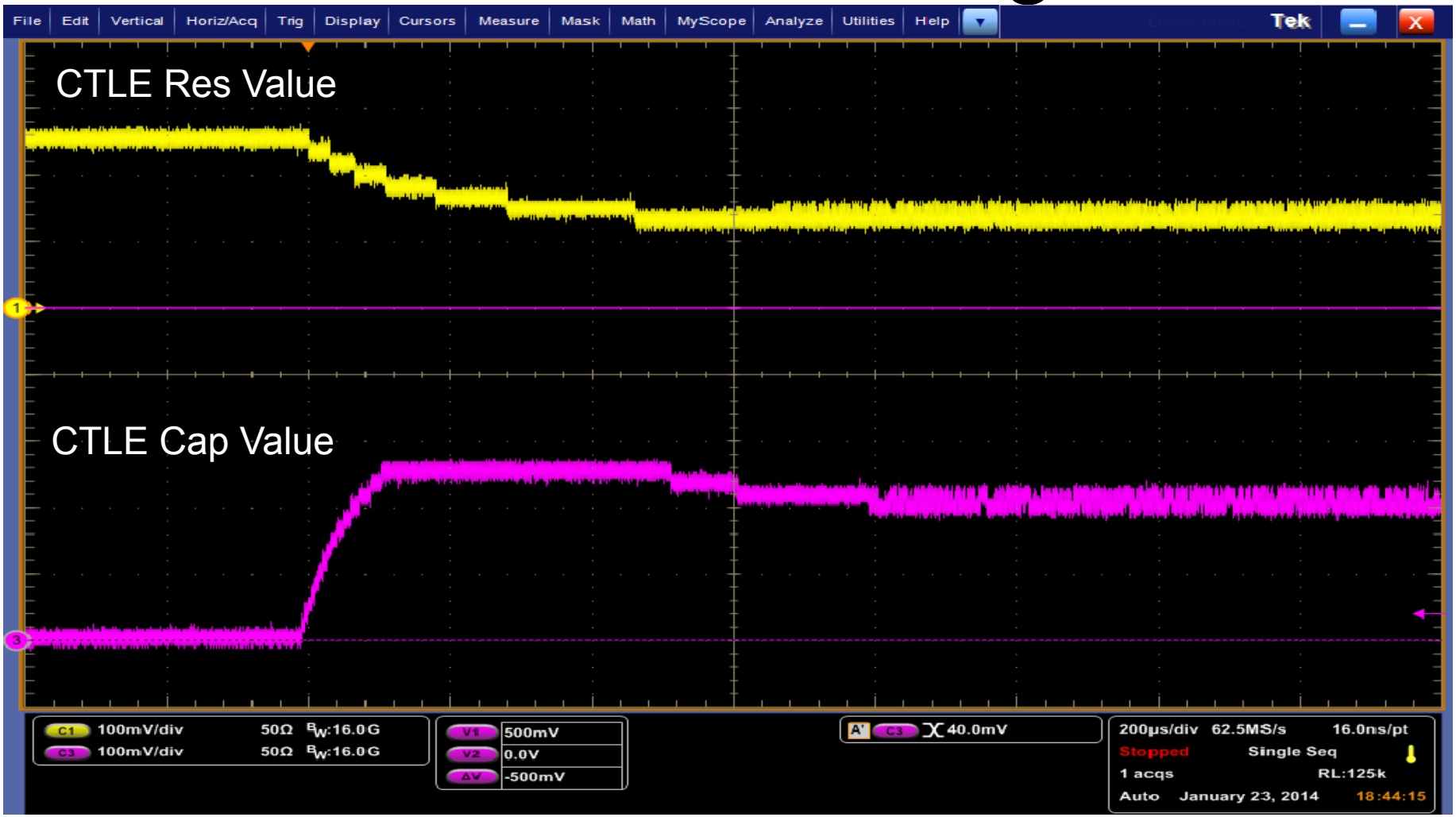
- RX performance over DFE taps

RX performance



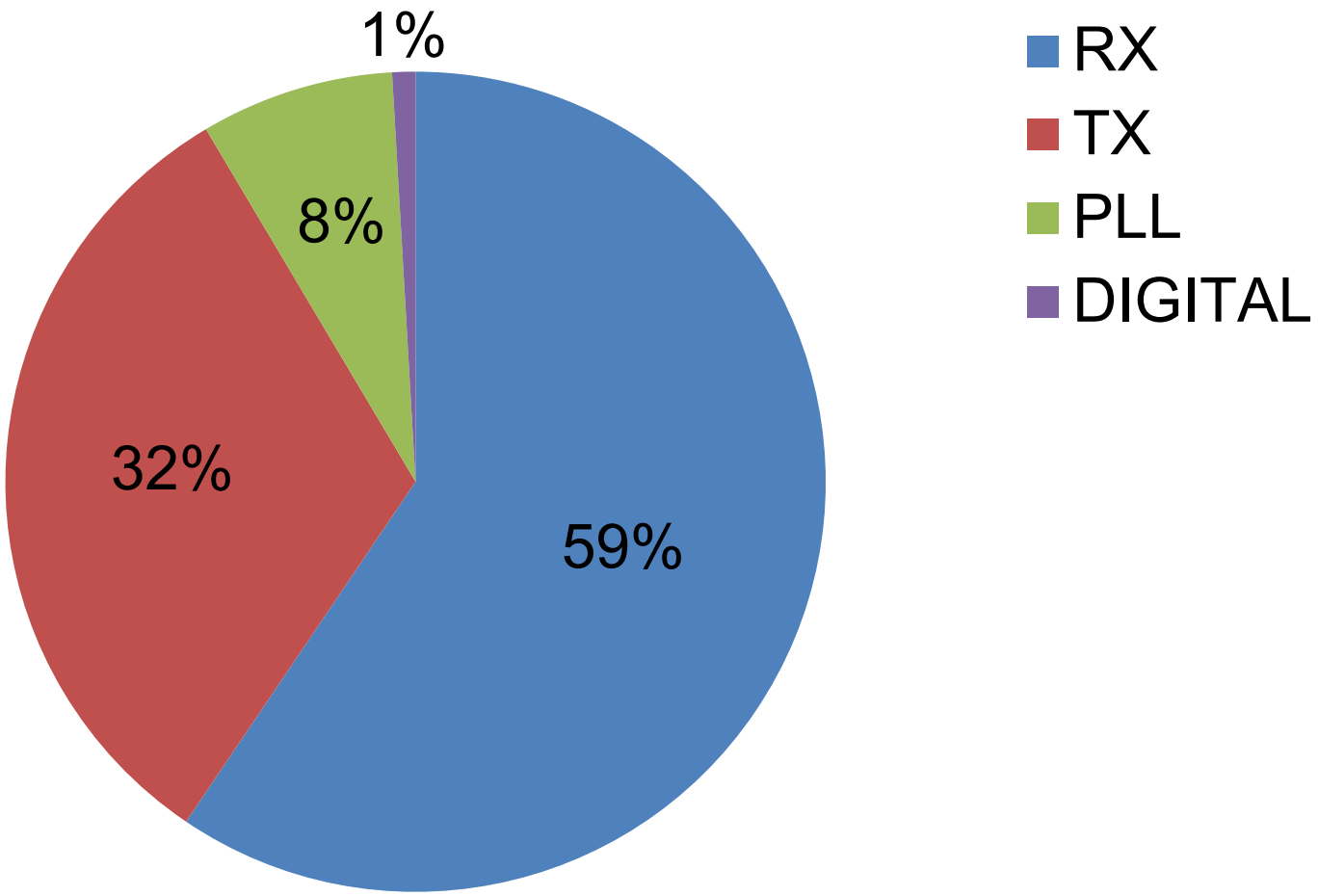
- 22Gb/s : 0.3UI eye opening at 10^{-12}
- 16Gb/s : 0.5UI eye opening at 10^{-12}

CTLE HF and LF gain



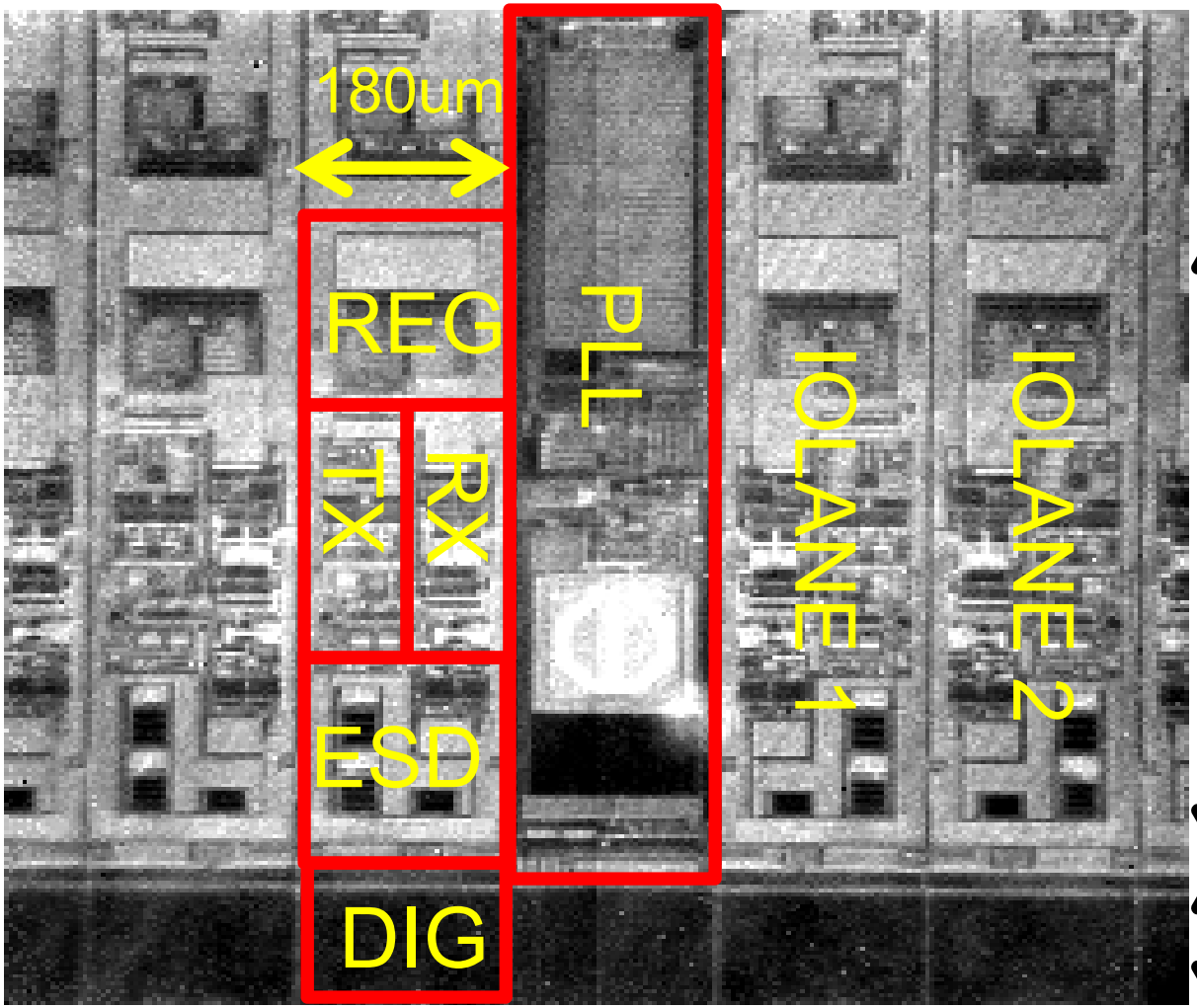
- CTLE LF and HF gain adaptation

Simplex Power breakdown



130mW Total Power for a 16 x 20Gb/s simplex link

IOLANE Die Photo



TX + RX Area :
0.18mm x 0.65mm

PLL + Bias Area :
0.18mm x 1.1mm

2x Digital Macro :
0.18mm x 0.27mm

Performance summary

Technology	28nm CMOS
Power Supply	1.35V / 0.9V
Area (1 PLL + 16 Lanes)	1.62mm x 1.6mm
Total bandwidth / IOBRICK	320Gb/s (16 x 20 Gbps)
Power Efficiency at 20Gb/s	6.5pJ/bit
BW / Perimeter	198Gbps/mm
LC-PLL closed loop BW	1.2 MHz
PLL jitter (100 kHz – 100 MHz)	420 fs, rms
LF, HF Gain range of CTLE	LF: -4 to 6 dB, HF : Up to10 dB
Power efficiency of RX CTLE	0.3pJ/bit
Power efficiency of RX samplers	0.4pJ/bit
Total TX/RX pad cap	550fF
Insertion loss capability	20dB
RX input-referred noise	0.9mV, rms

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- Silicon Results
- Conclusion

Conclusion

- A 16 x 20Gb/s serial link transceiver with 1-tap FFE, 2-tap DFE and IIR has been demonstrated
- Single stage CTLE with TIA output stage is implemented with over 10dB boost
- Direct feedback of all DFE taps to reduce power and area
- Edge DFE, H_X is applied to improve CDR
- Measured link BER < 10^{-15} with PRBS 31 pattern

Acknowledgements

- Special thanks to
  - B. Simms, D. Herrig, and H. Choi for chip bring up
  - S. Sudhakaran, S. Hwang and F. Lambrecht for SI simulations
  - A. Gupta, R. Gummadi, and R. Newcomb for link architecture discussions
  - A. Yang, M.Patel, B. Beecher, P.Gordon for chip layout

A 205mW 32Gb/s 3-Tap FFE/ 6-Tap DFE Bidirectional Serial Link in 22nm CMOS

James Jaussi, Ganesh Balamurugan, Sami Hyvonen, Tzu-Chien Hsueh, Tawfiq Musah, Gokce Keskin, Sudip Shekhar*, Joseph Kennedy, Shreyas Sen, Rajesh Inti, Mozhgan Mansuri, Michael Leddige, Bryce Horine, Clark Roberts, Randy Mooney, Bryan Casper

Intel, Hillsboro, OR

*now with University of British Columbia, Vancouver, Canada

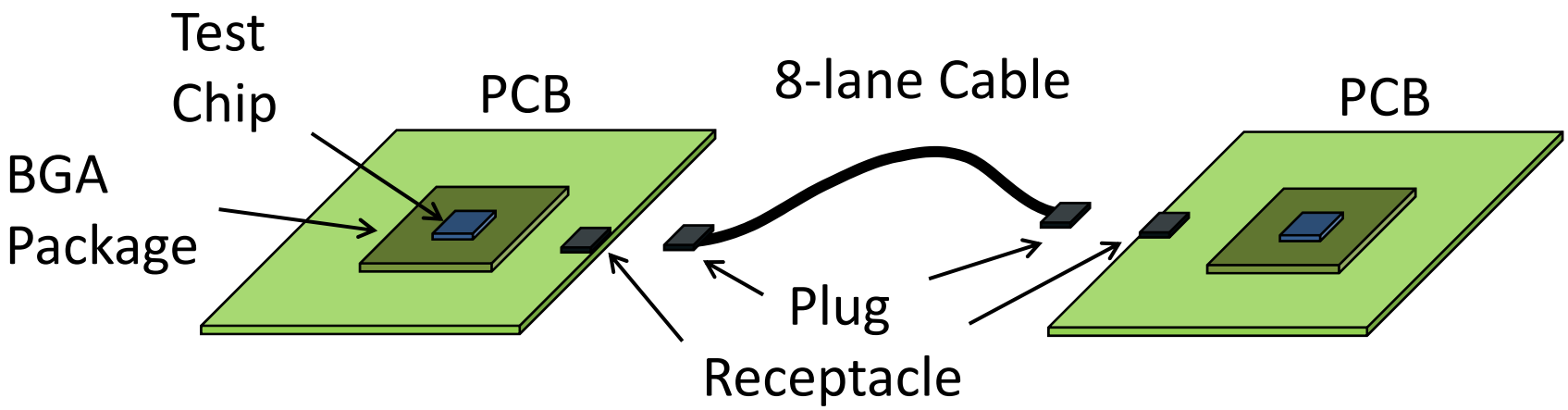
Outline

- Motivation
- Link architecture
- Circuit implementation
- Prototype measurements
- Conclusion

Motivation

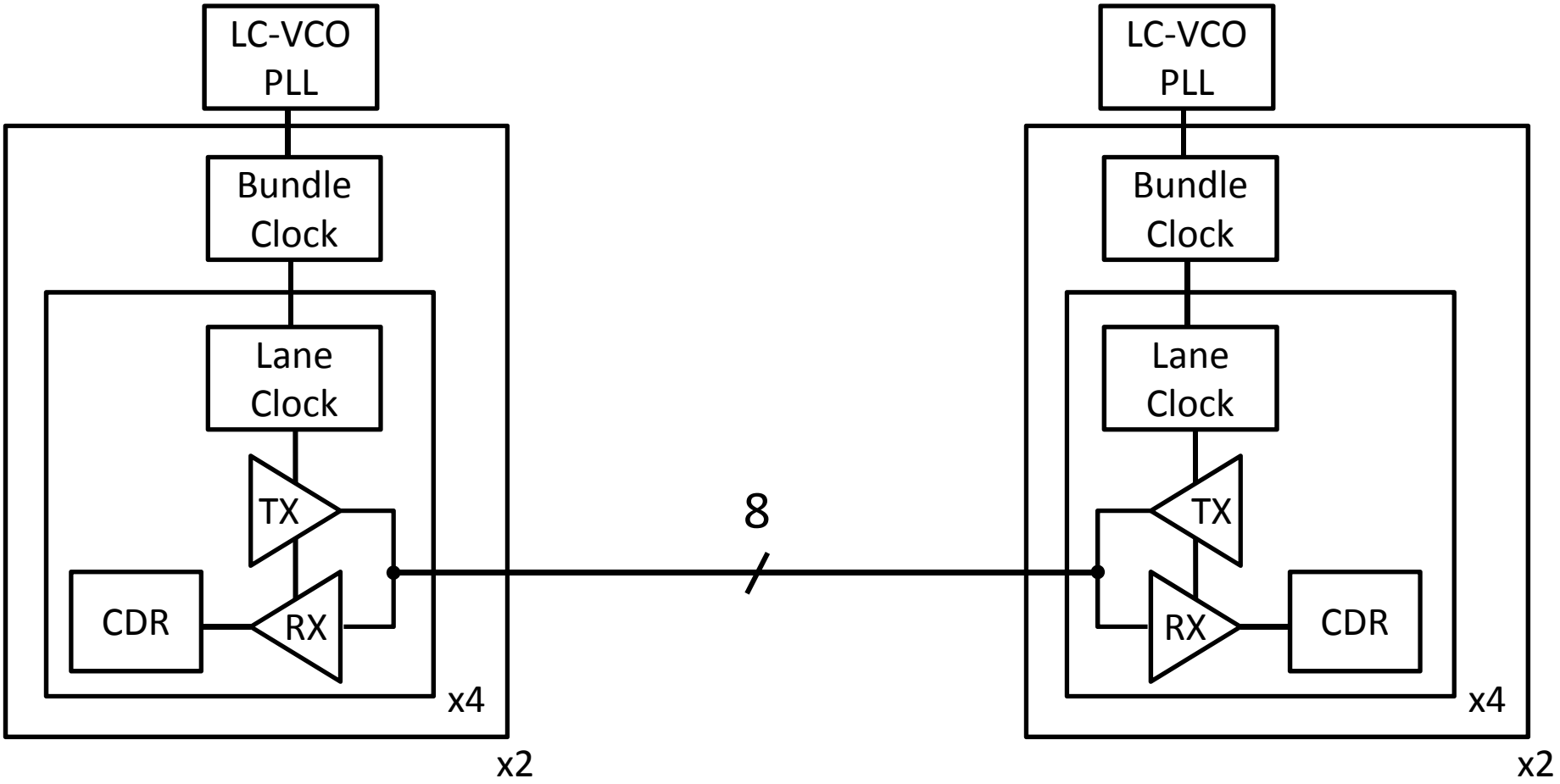
- Serial I/O bandwidth demand continues to increase
- Low-cost, low-power serial link needed

Interconnect Topology



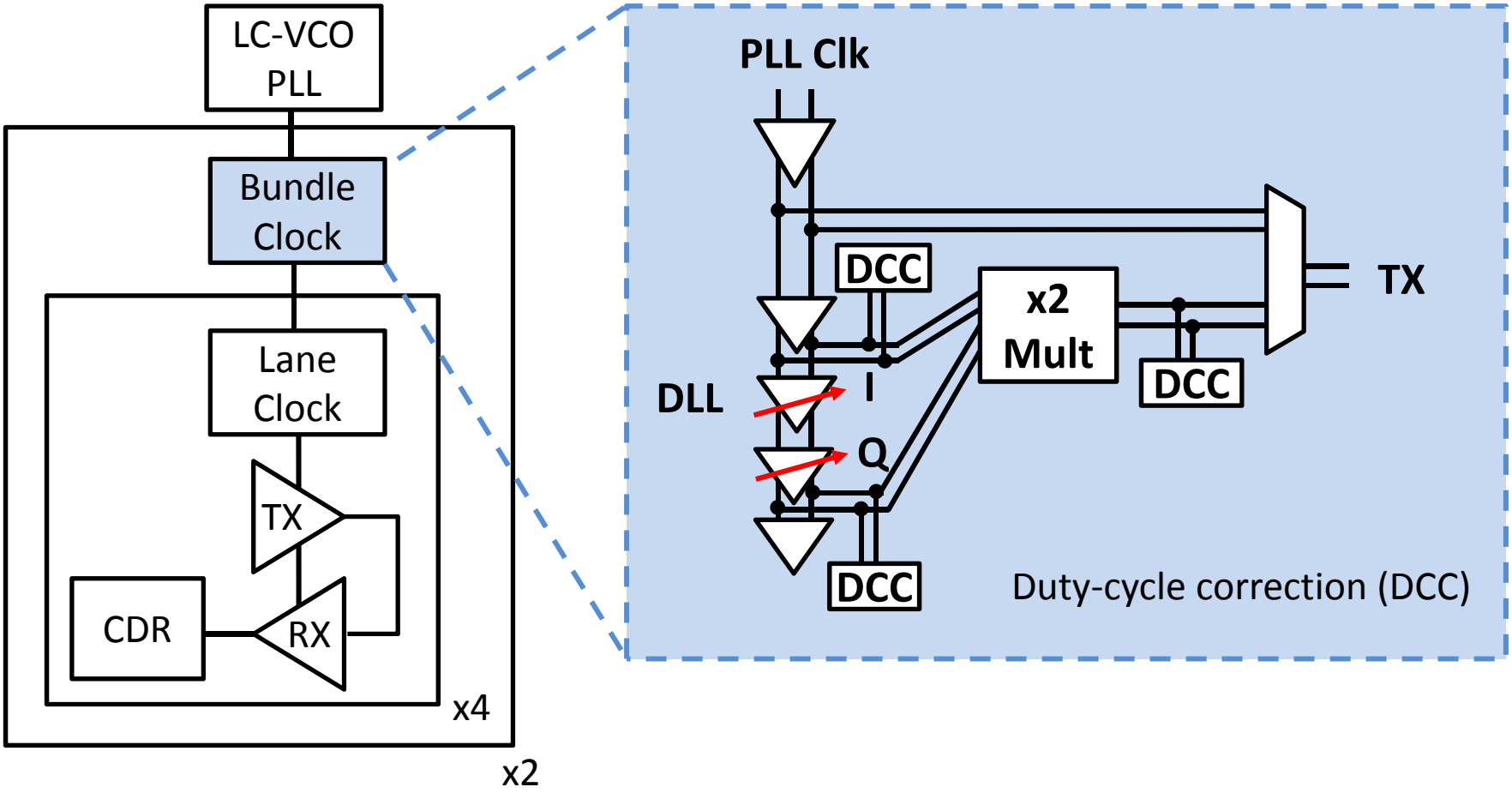
- Low-profile connector: 3mm height
- Target cable assembly loss: <15dB
- Bandwidth scalable for multiple generations

Link Architecture



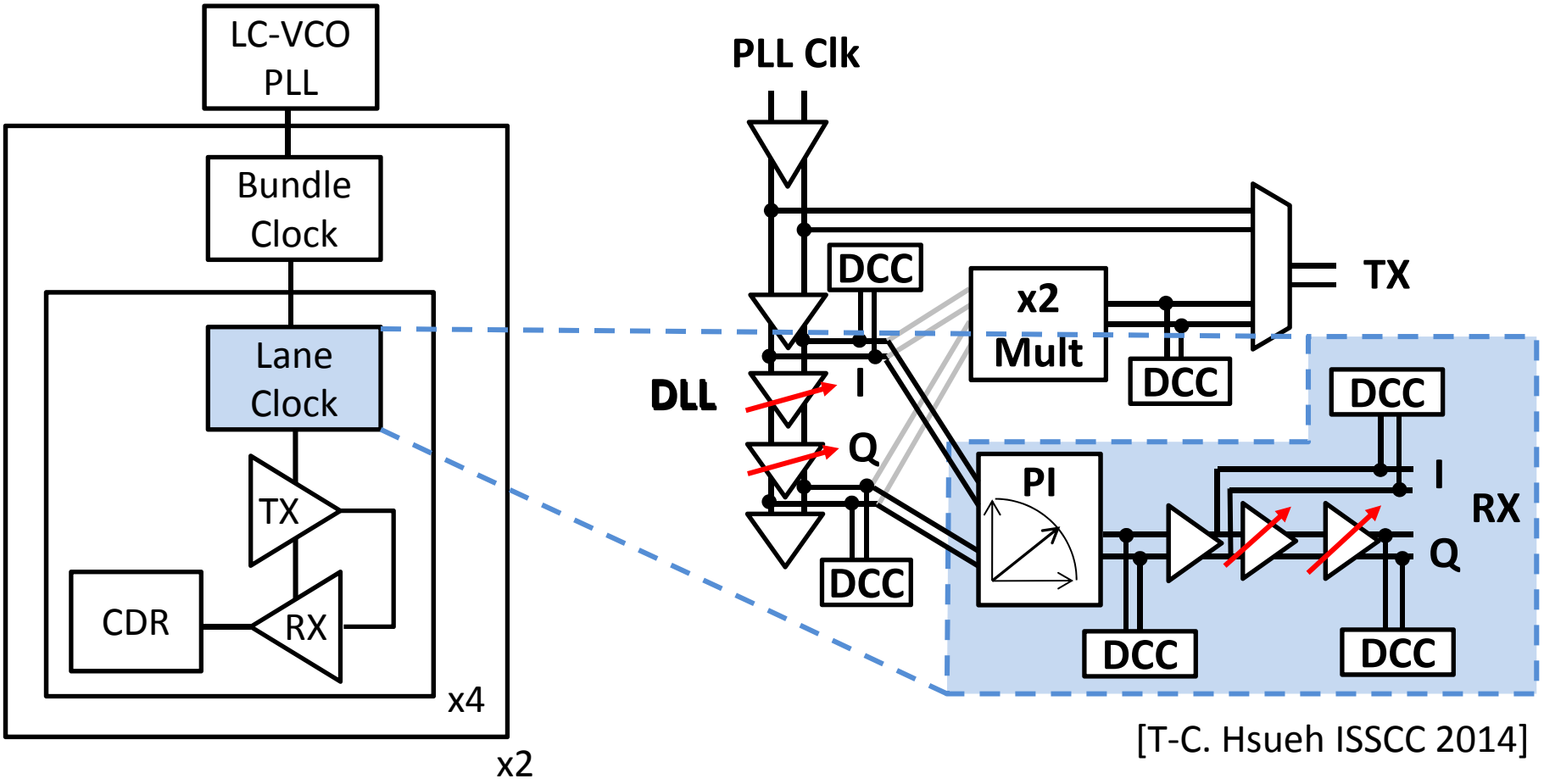
- Bundle clock to amortize clocking power
- 8 bidirectional lanes

Bundle Clock



- Regulated CMOS clocking
- Scalable quarter-rate clock frequency: 2GHz to 8GHz

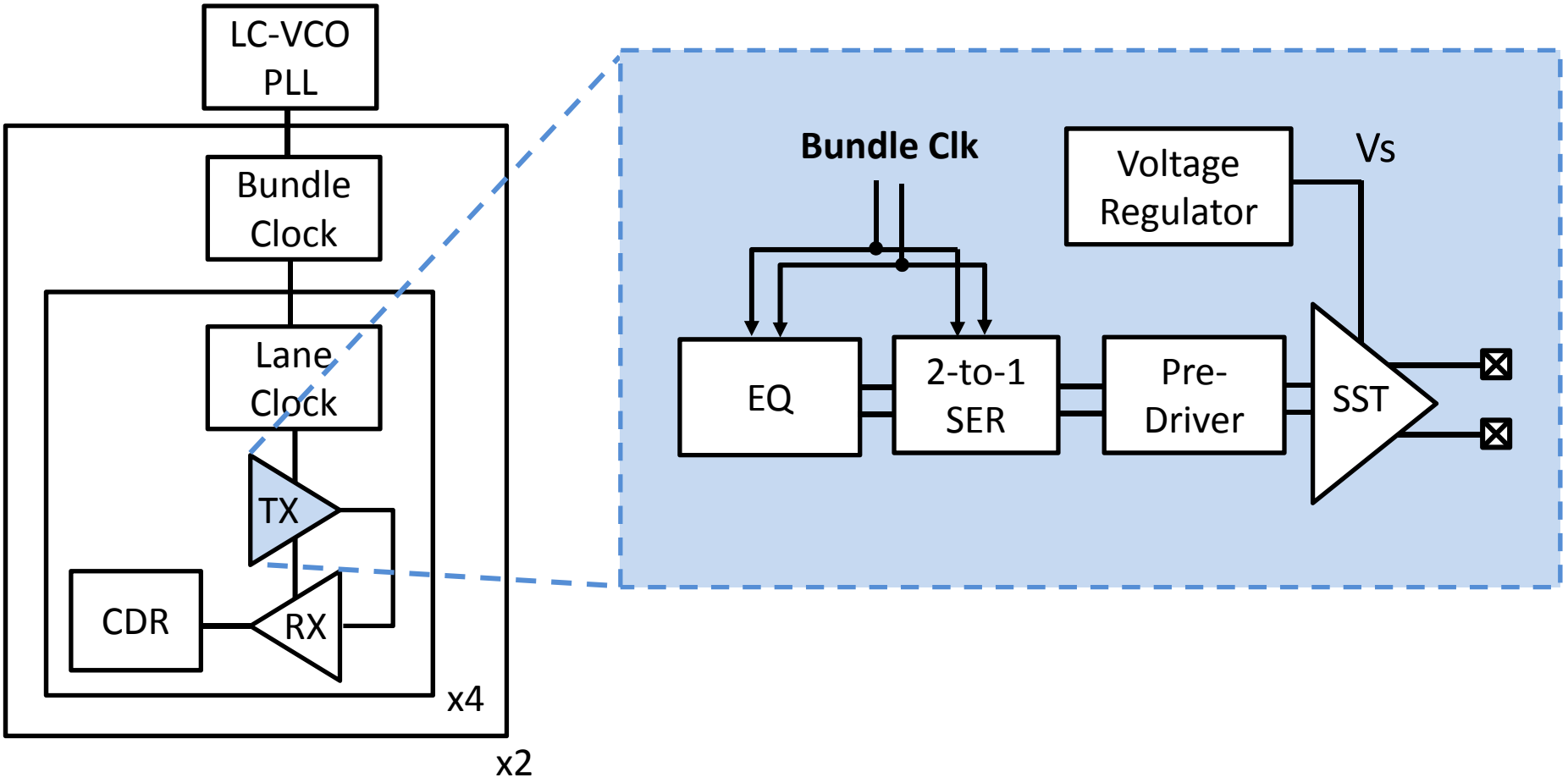
Lane Clock



[T-C. Hsueh ISSCC 2014]

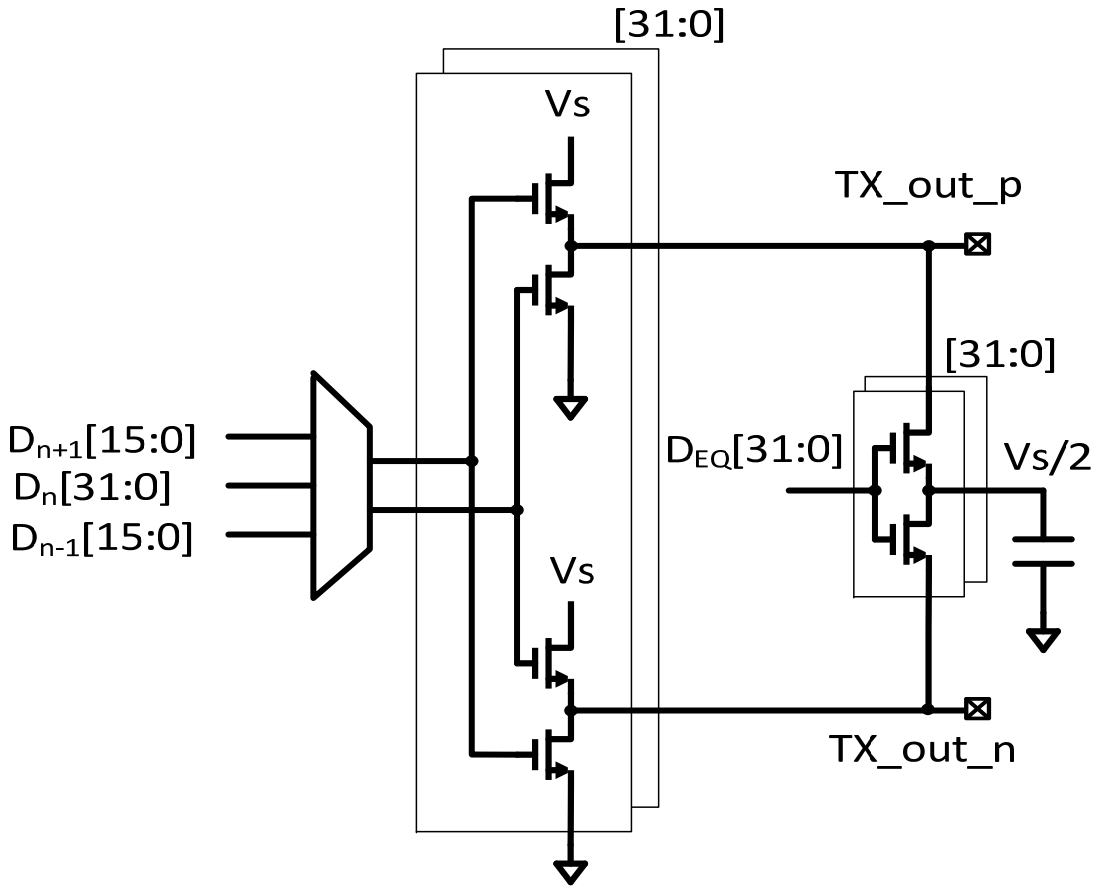
- Quadrature PI with continuous DCC
- I/Q phases with DCC and quadrature correction

Transmitter



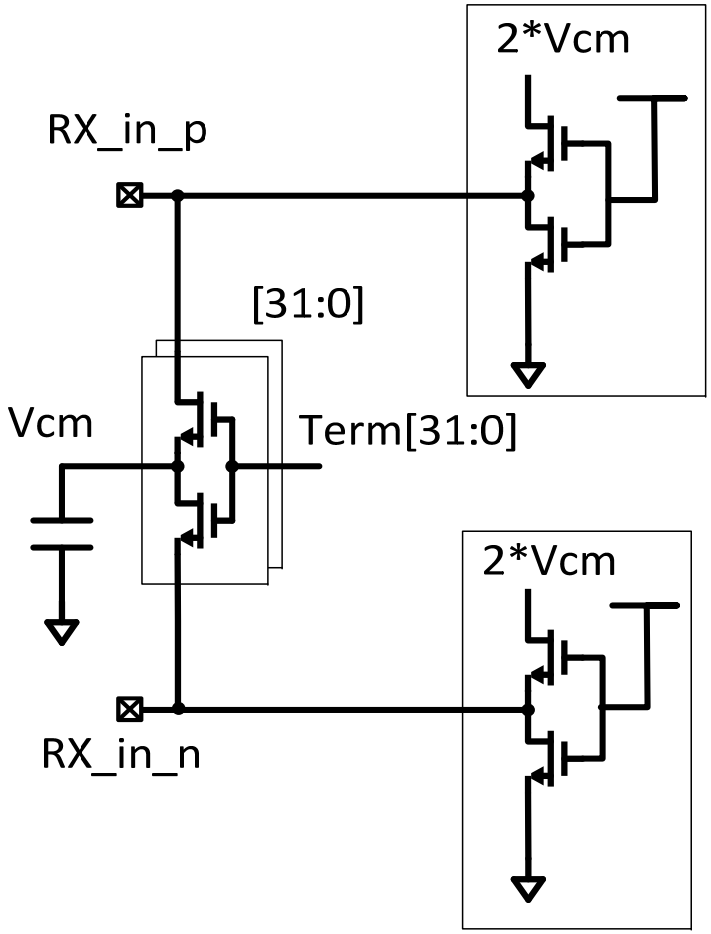
- Source-series terminated (SST) 3-tap FFE
- Dual-mode driver

Dual-mode Driver: TX



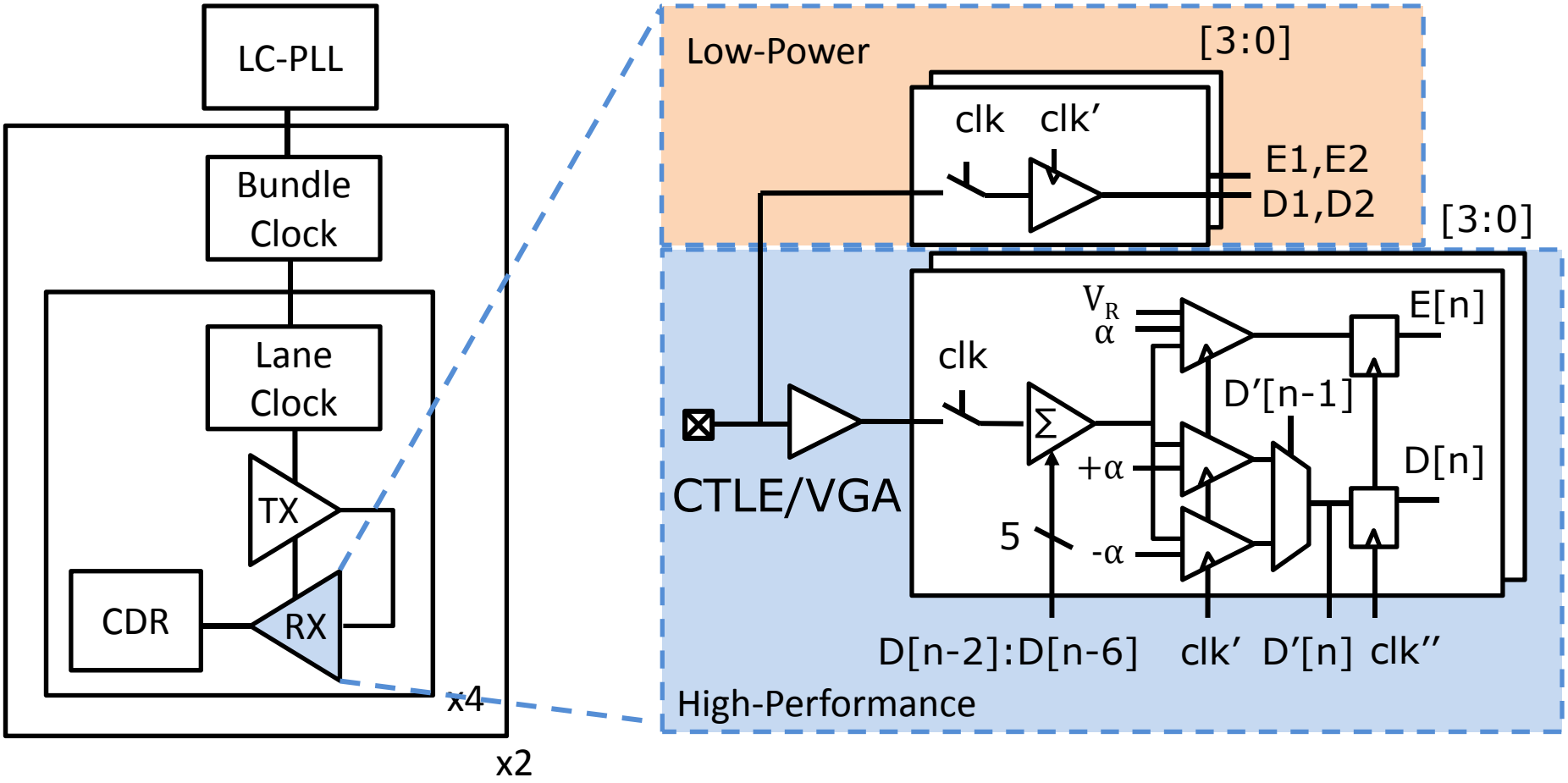
- Push/pull NMOS driver
- Shorting devices for equalization

Dual-mode Driver: RX Termination



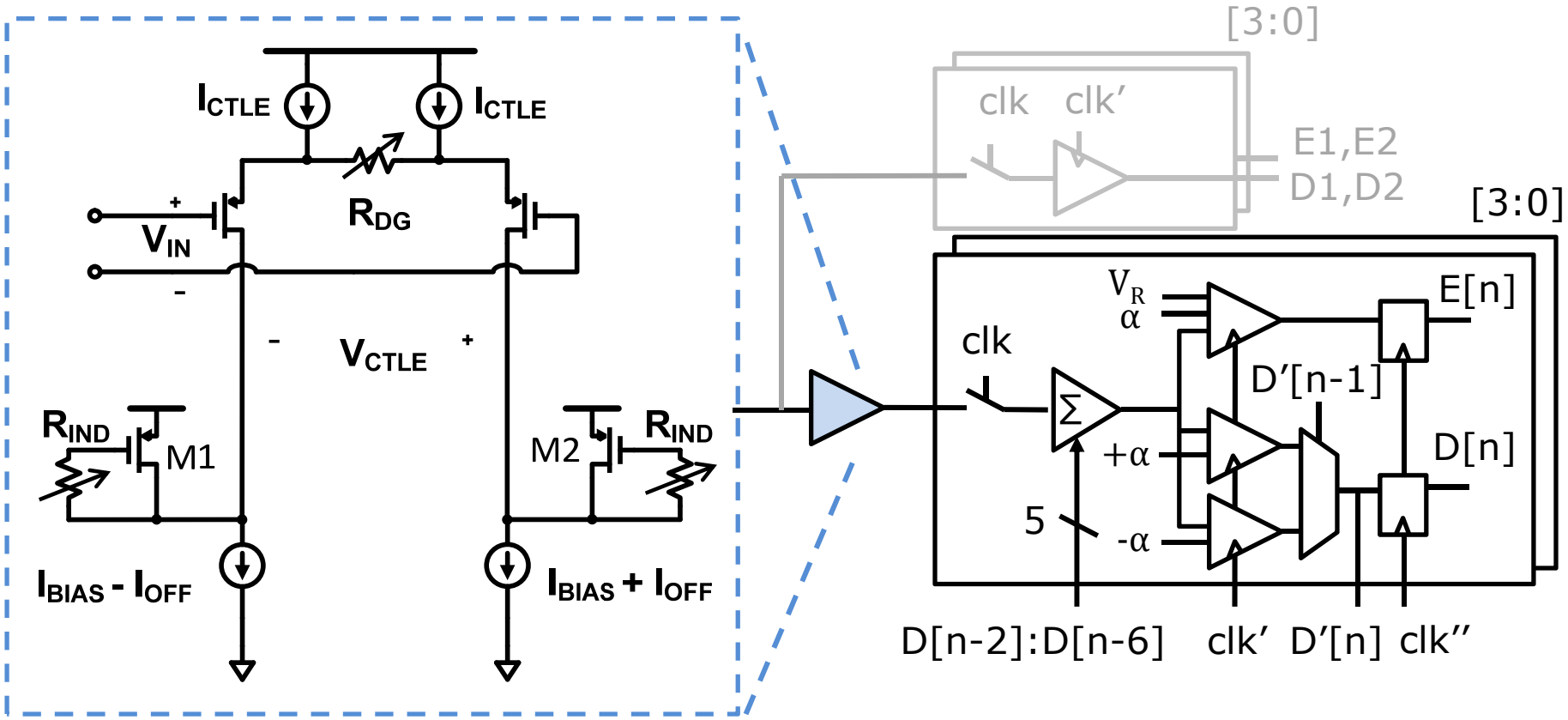
- Equalizing devices repurposed for channel termination
- Driver devices repurposed for common-mode voltage

Receiver Front-End



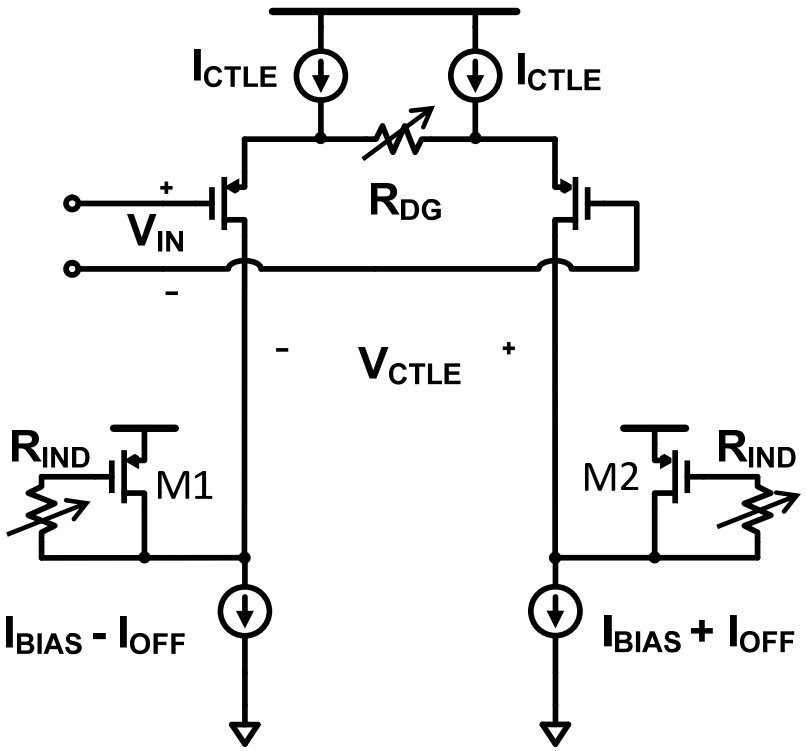
- Dual-mode RX FE: low-power and high-performance
- 1st order CTLE and 6-tap DFE

1st Order CTLE

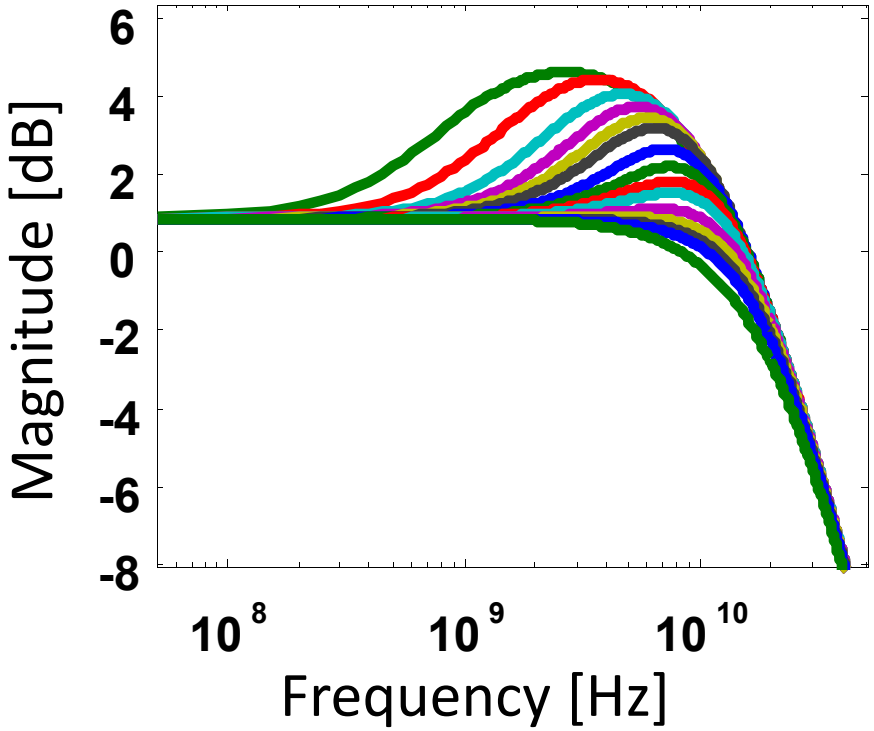


- Active inductor to minimize die area
- Independent control of peaking and VGA

CTLE Frequency Response

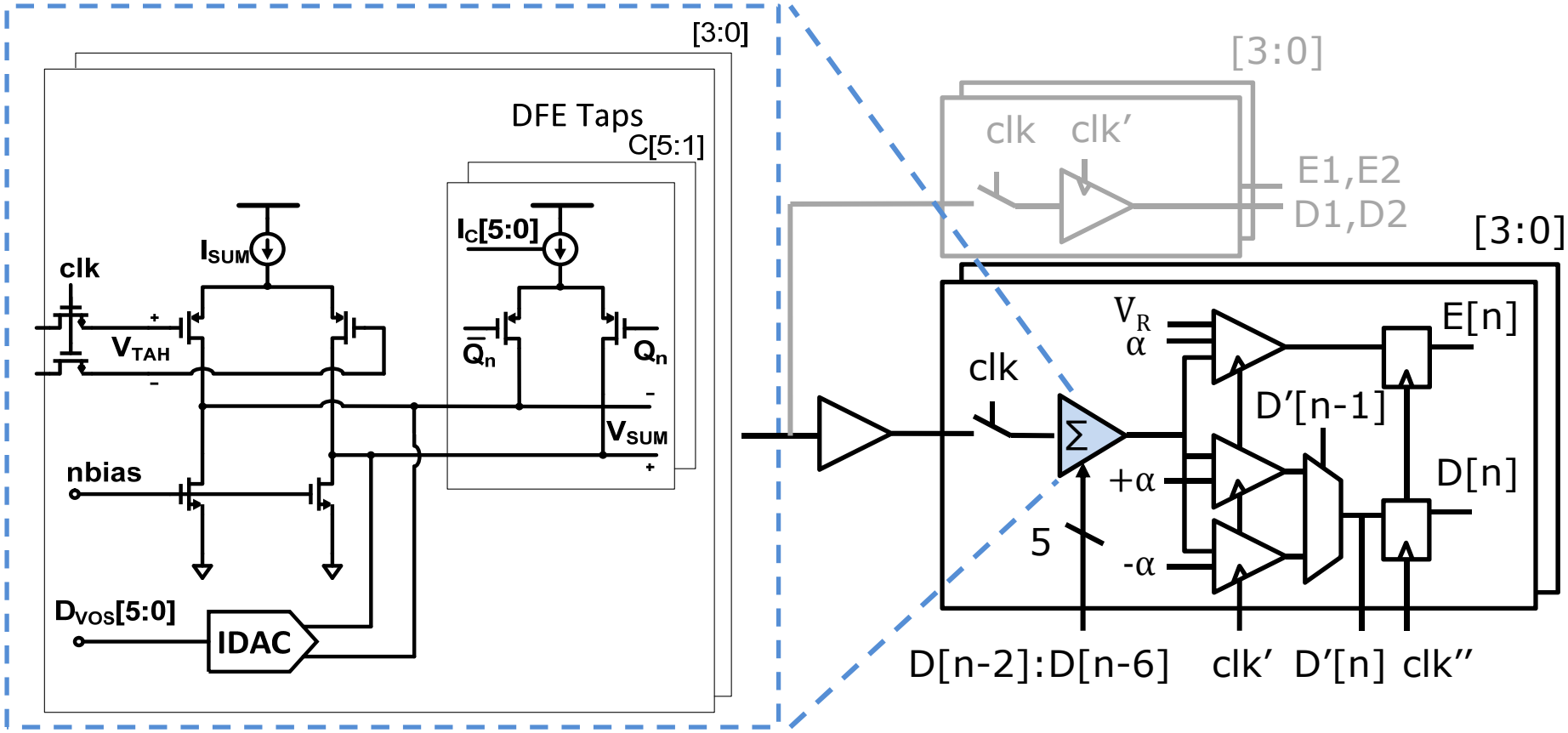


Simulated Frequency Response



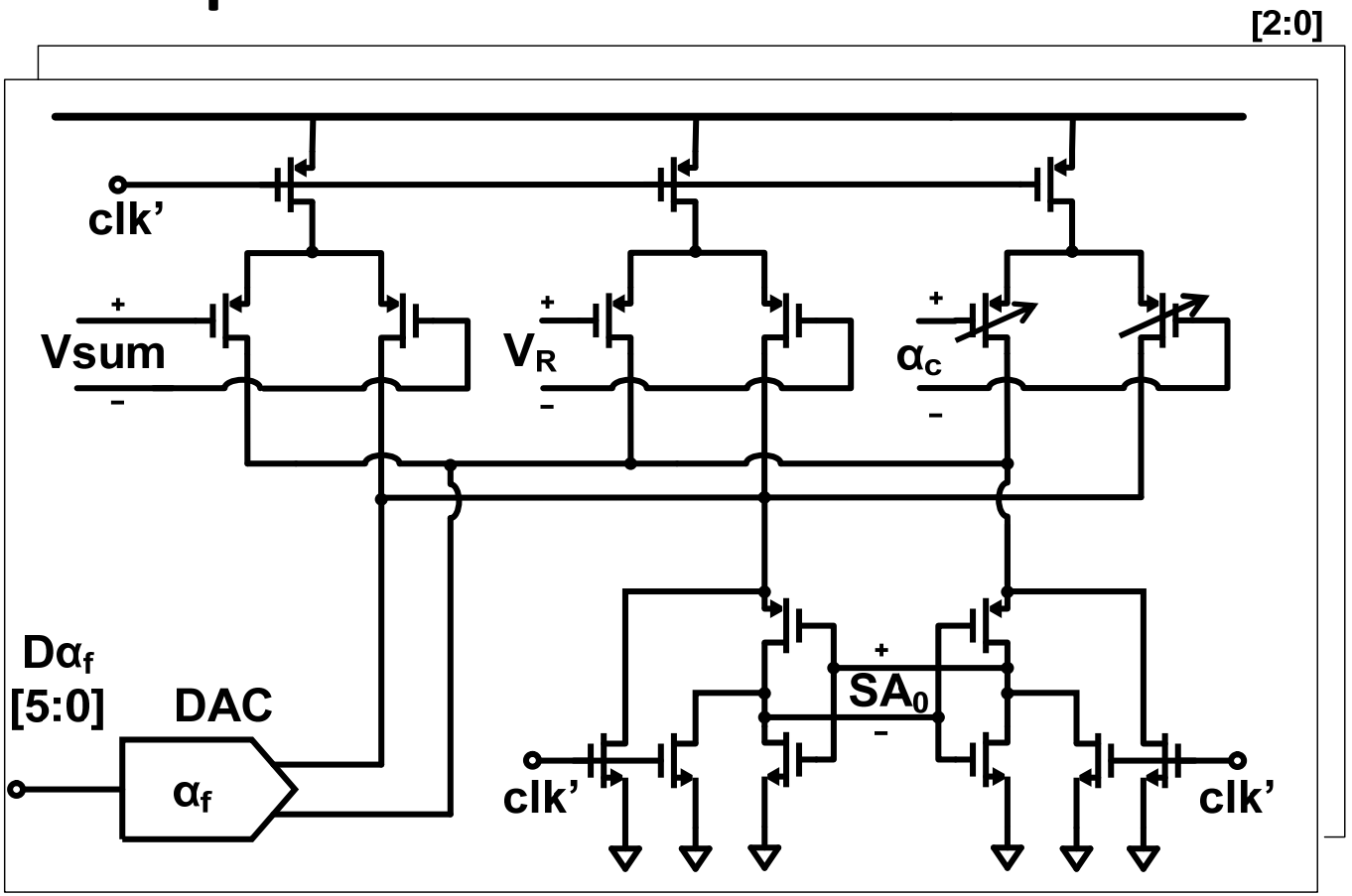
- CTLE peaking ranges from 0dB to 4dB
- Variable R_{DG} controls CTLE gain

DFE Summer



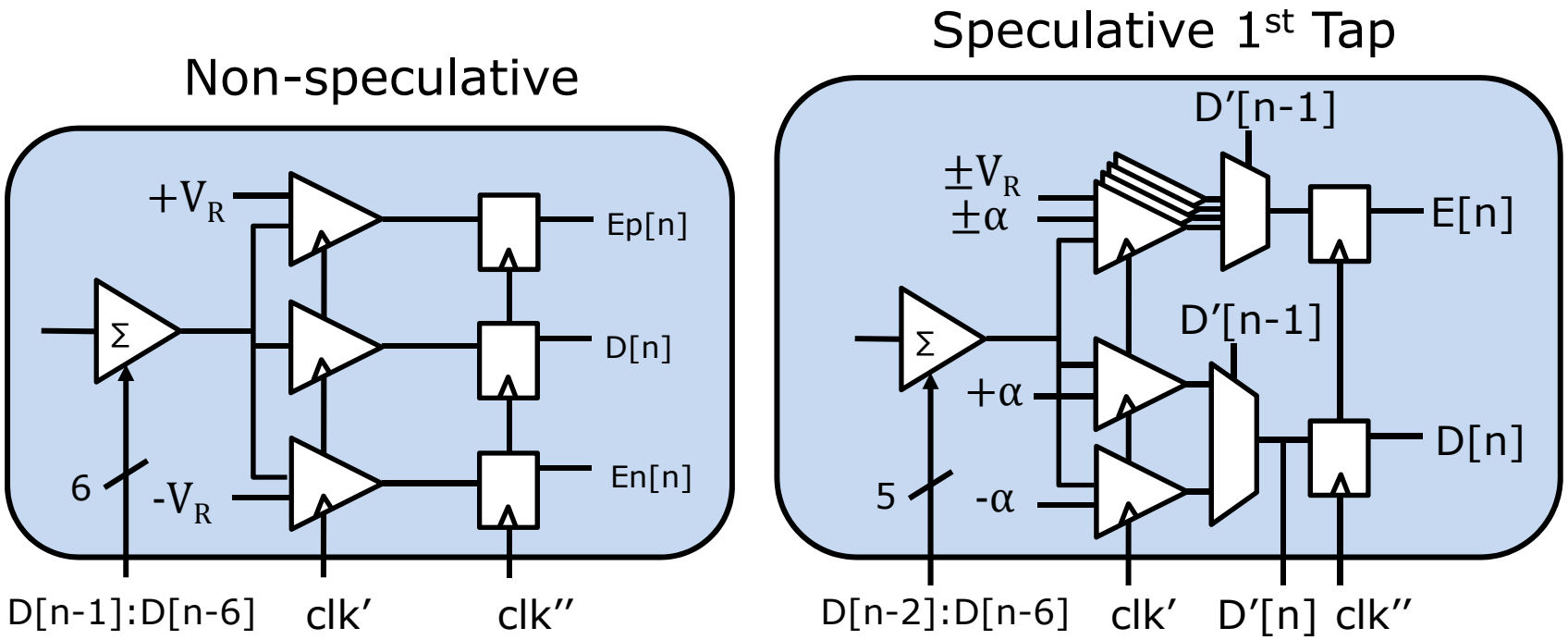
- CML DFE summer
- Scalable date rate: 4 - 32Gb/s

Speculative DFE Latch



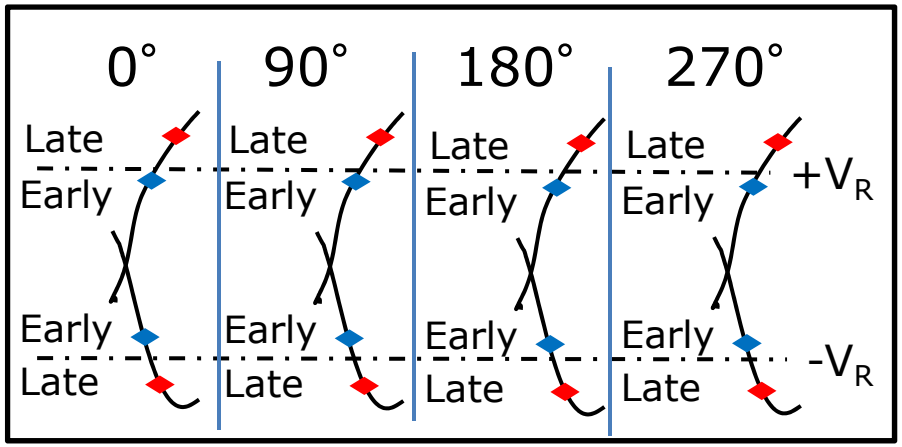
- 3-input latch: summer output, speculative tap and reference voltage

Baud-Rate Clock Recovery and DFE



- Speculative tap doubles number of comparators for baud-rate phase detection

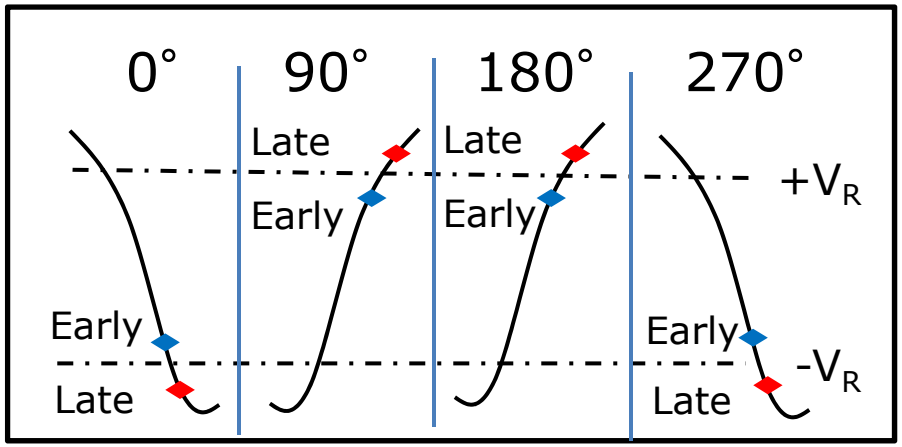
Conventional Phase Detection



Phase Sample	Ref. Voltage	1st Tap	Valid Pattern D[n:n+1]
0°	$\pm V_R$	$\pm\alpha$	10 or 01
90°	$\pm V_R$	$\pm\alpha$	10 or 01
180°	$\pm V_R$	$\pm\alpha$	10 or 01
270°	$\pm V_R$	$\pm\alpha$	10 or 01

- All edge transitions are detected
- Common requirement: phase error before and after edge have same early/late indication

Conditional Phase Detection

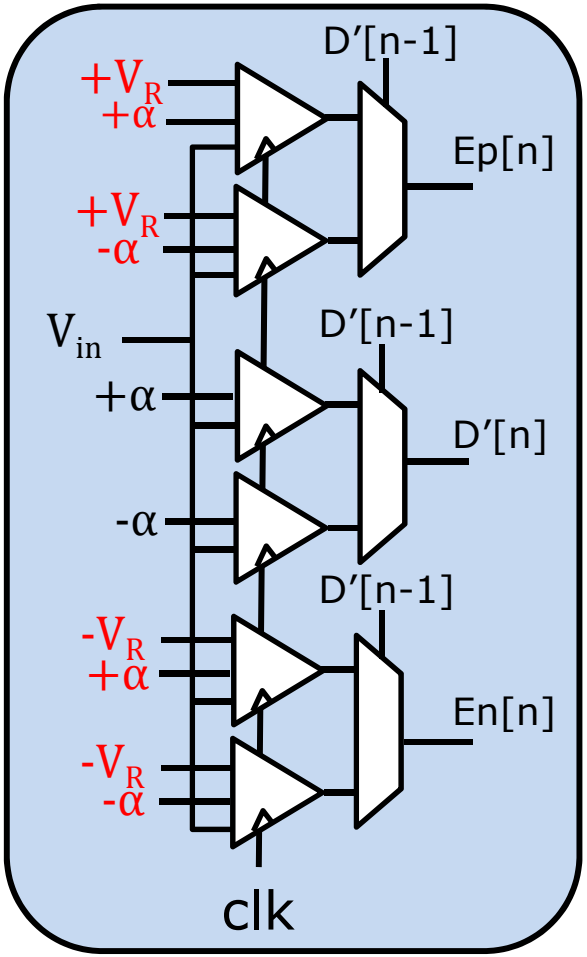


Phase Sample	Ref. Voltage	1st Tap	Valid Pattern D[n-1:n+1]
0°	-V_R	-α	100
90°	+V_R	+α	011
180°	+V_R	+α	011
270°	-V_R	-α	100

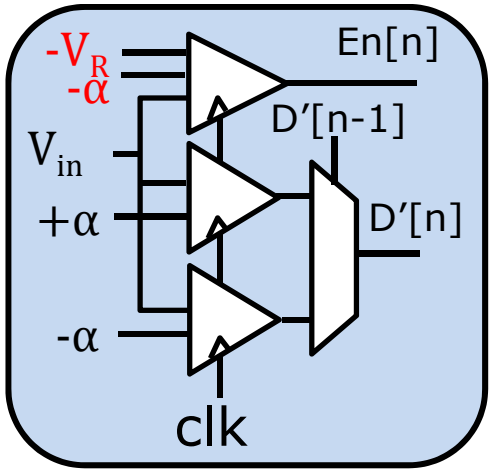
- Conditional pattern: after edge transition, two consecutive 1's or 0's
- Result: reduces number of possible valid edges by 75%
- Advantage: reduces number of comparators by 50%

Conventional Vs. Conditional FE

Conventional FE

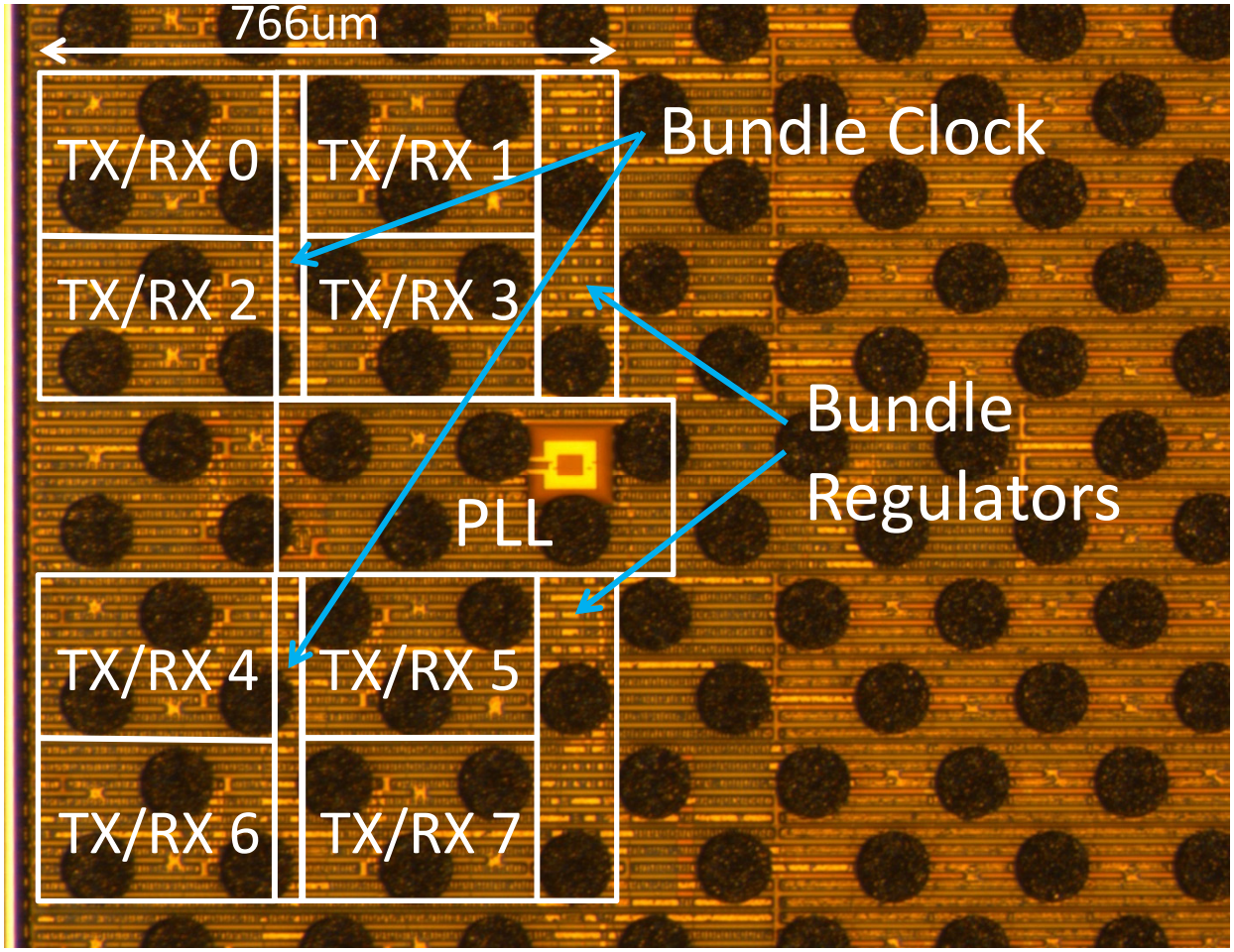


Conditional FE



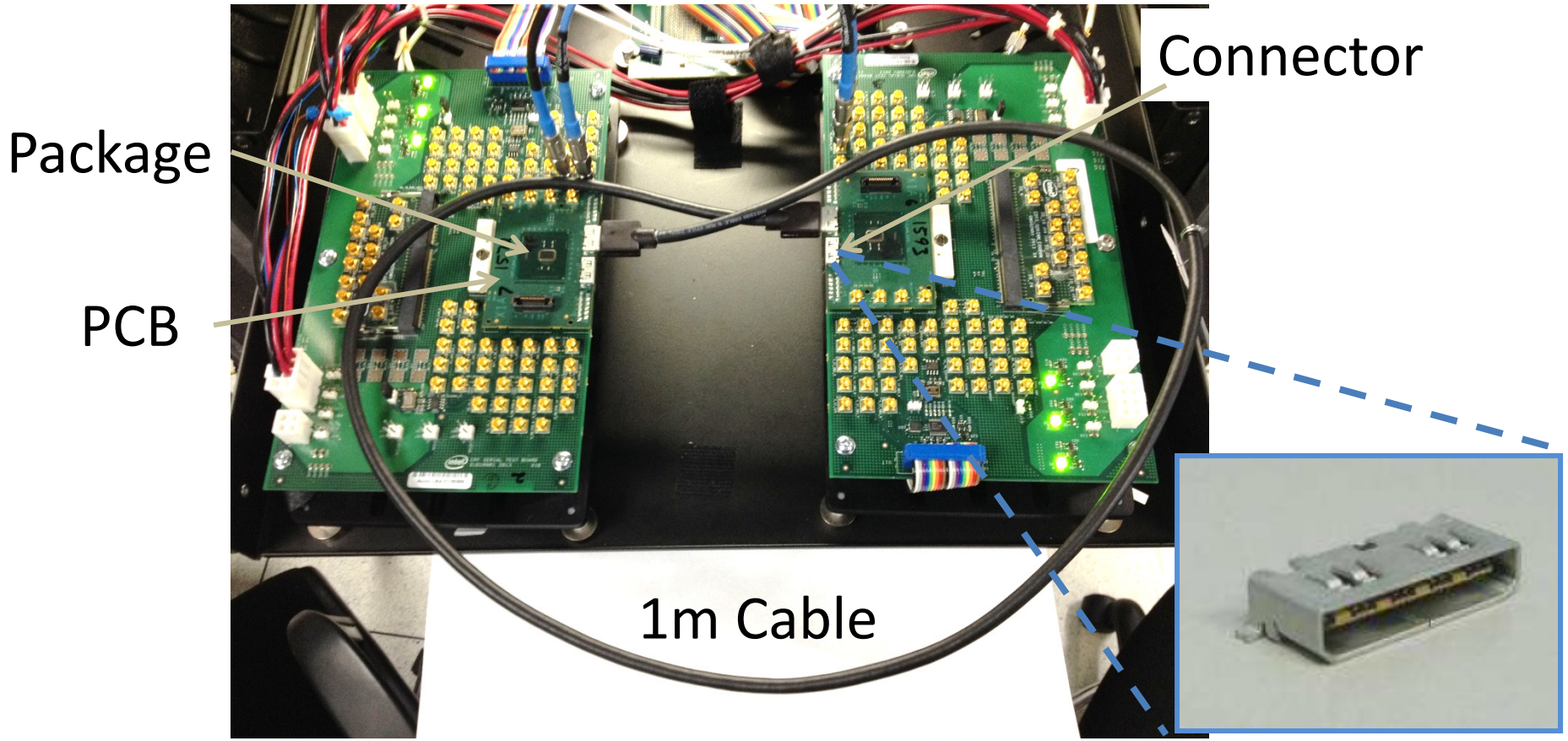
- 50% reduction in comparators

22nm CMOS Test Chip

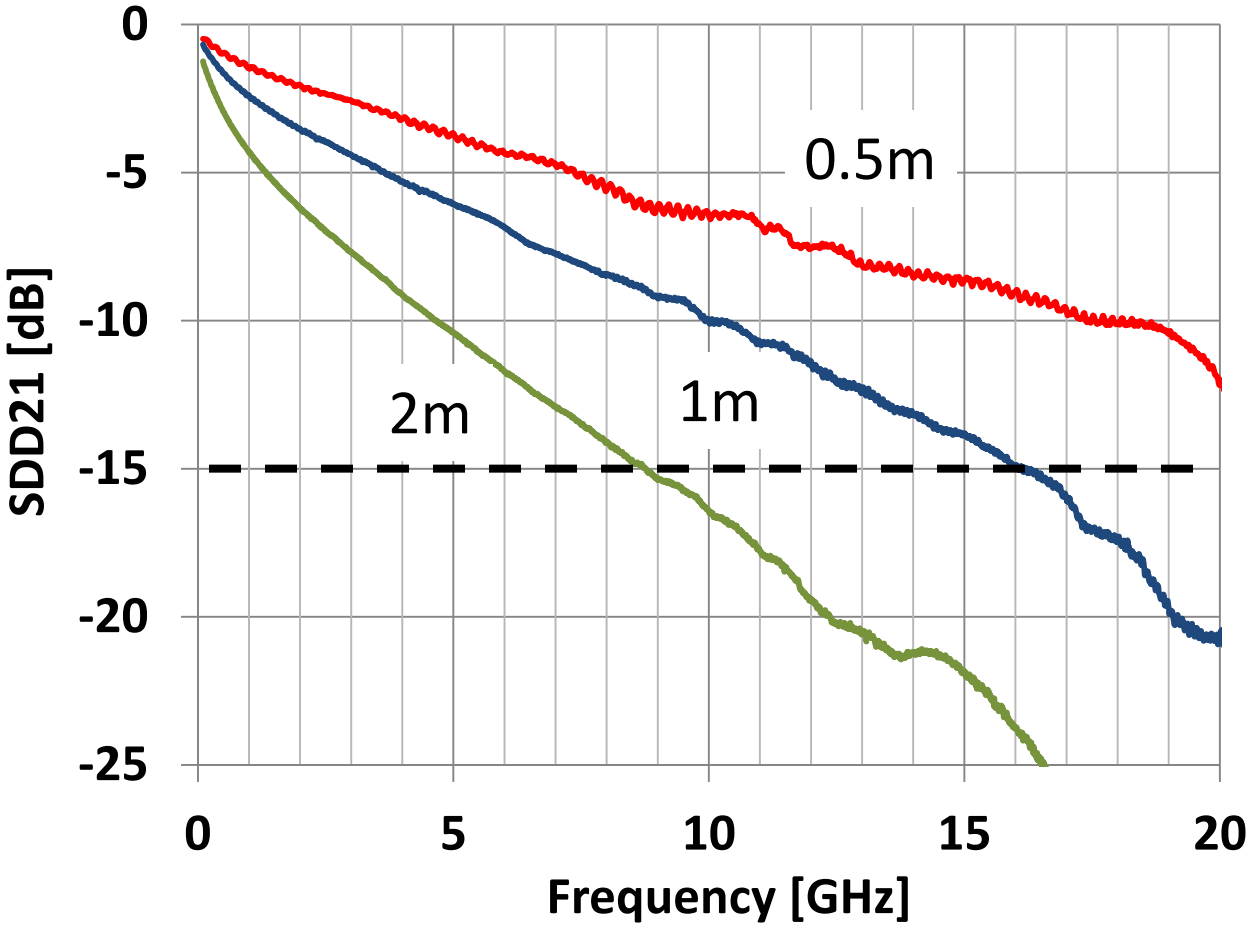


- TX/RX area: 0.079mm^2

Test Setup

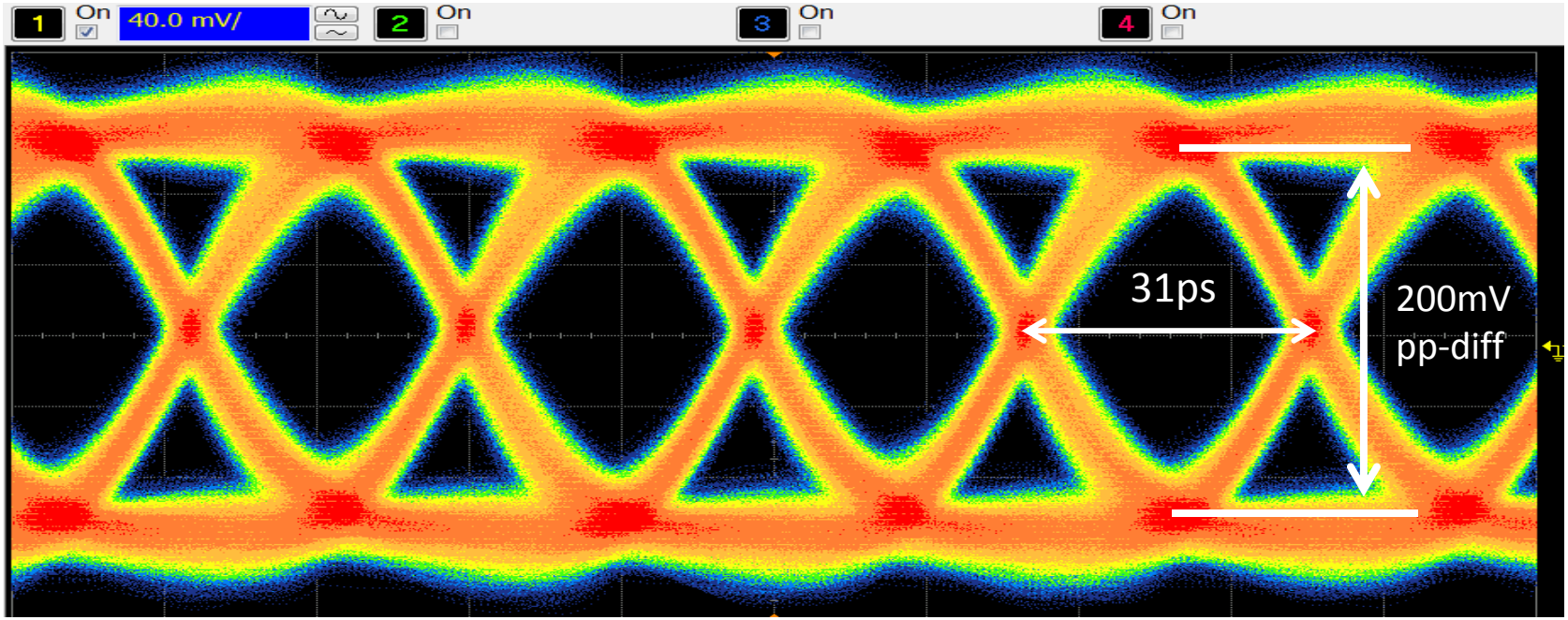


Measured Cable Assembly Loss



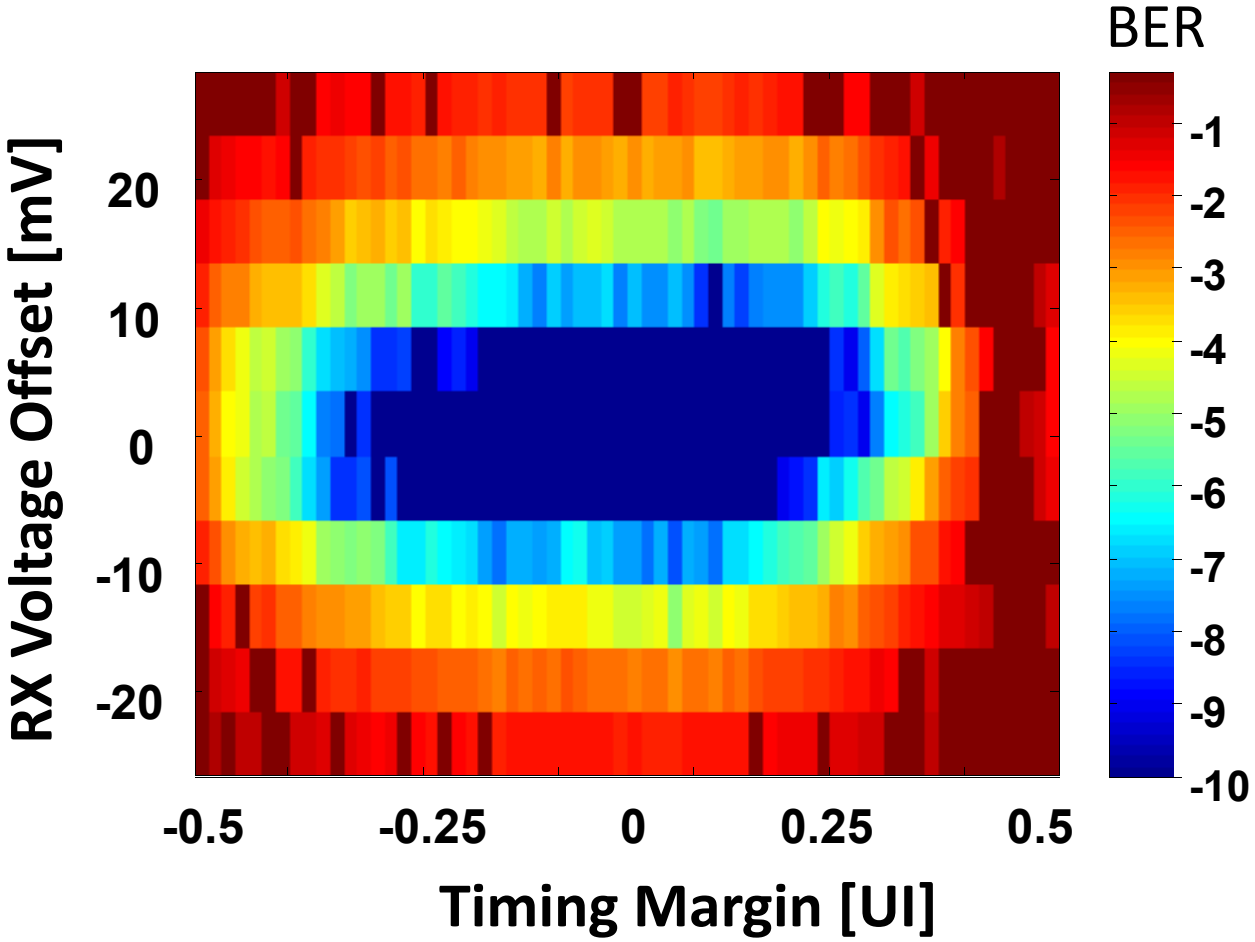
- Cable: 32AWG copper twisted-pair
- Target cable assembly loss: <15dB

Measured TX Waveform @32Gb/s



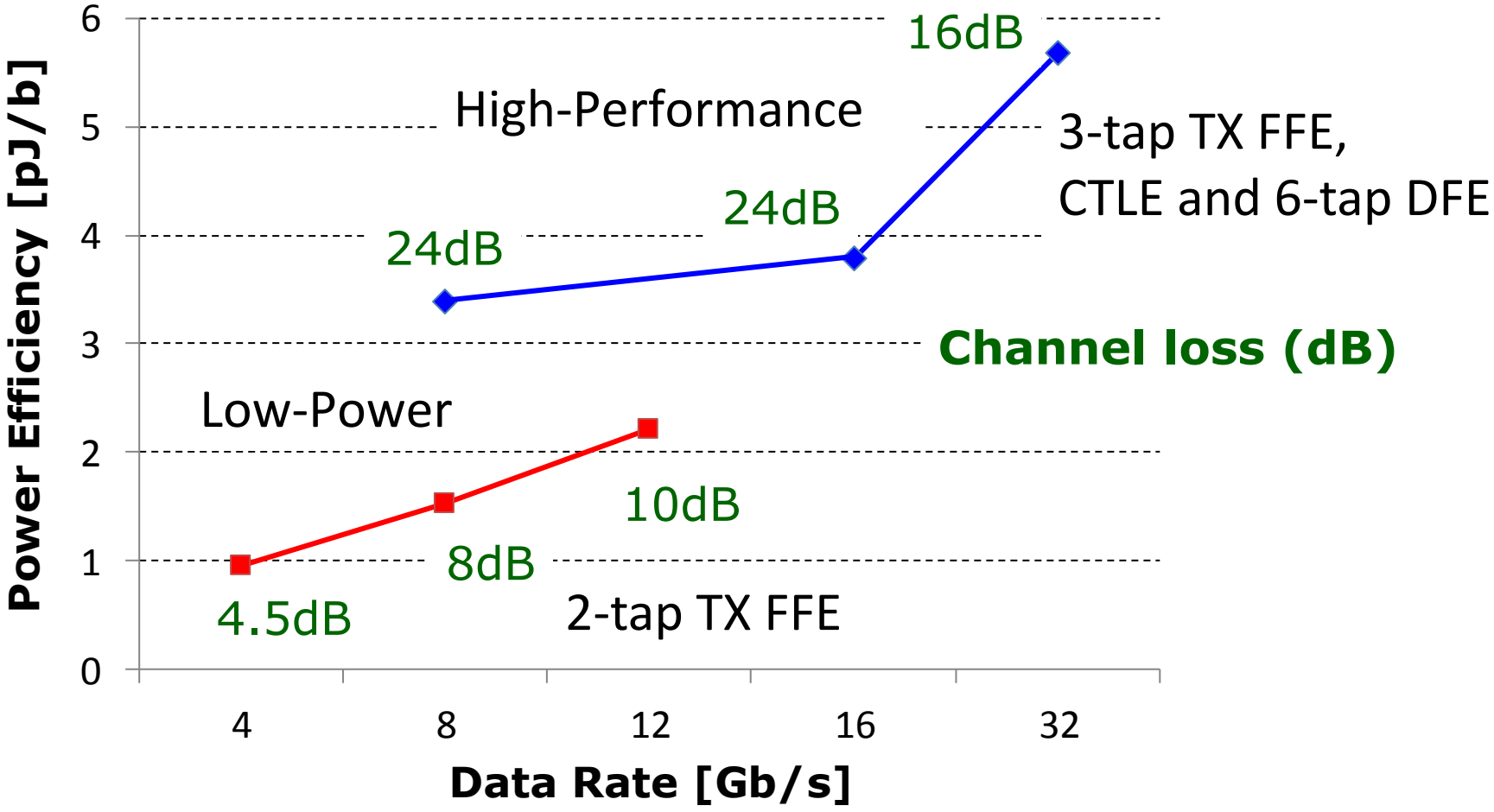
- Channel length: 2cm
- Transmit voltage: 200mV$_{pp\text{-}diff}$

On-die Measured BER Eye @32Gb/s



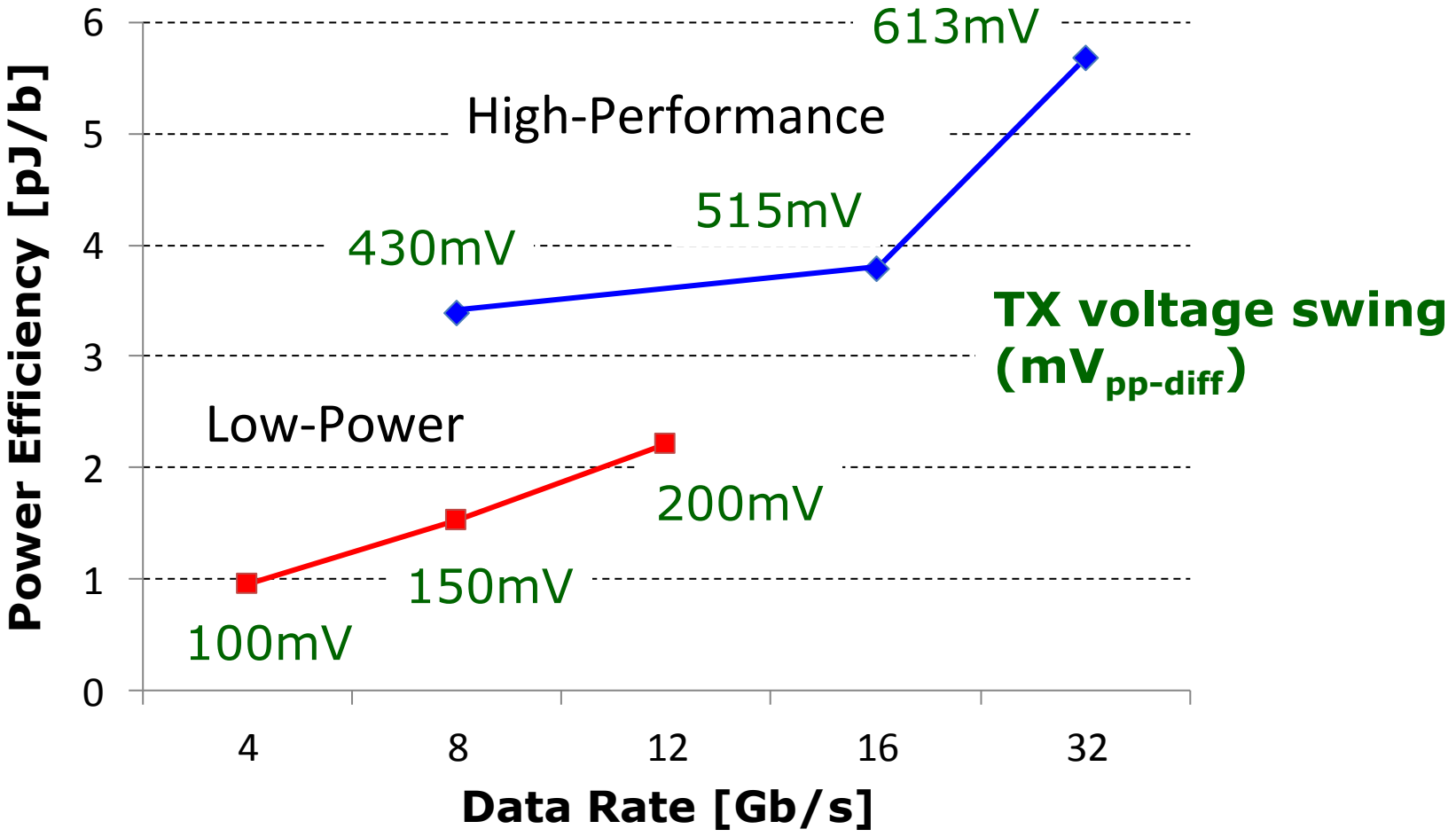
- Cable length: 0.5m
- PRBS10 data

Measured Power Efficiency



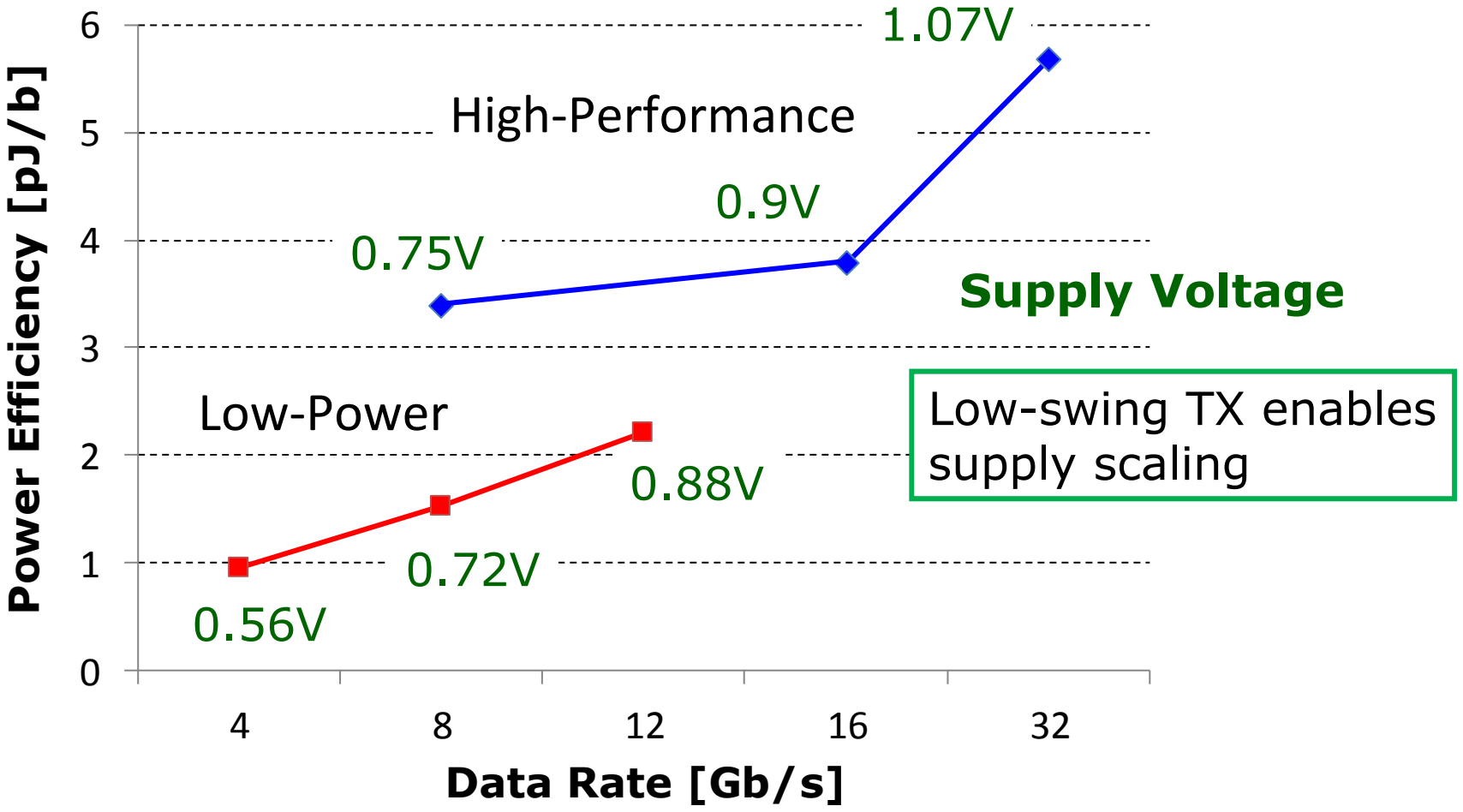
(PLL power not included)

Measured Power Efficiency



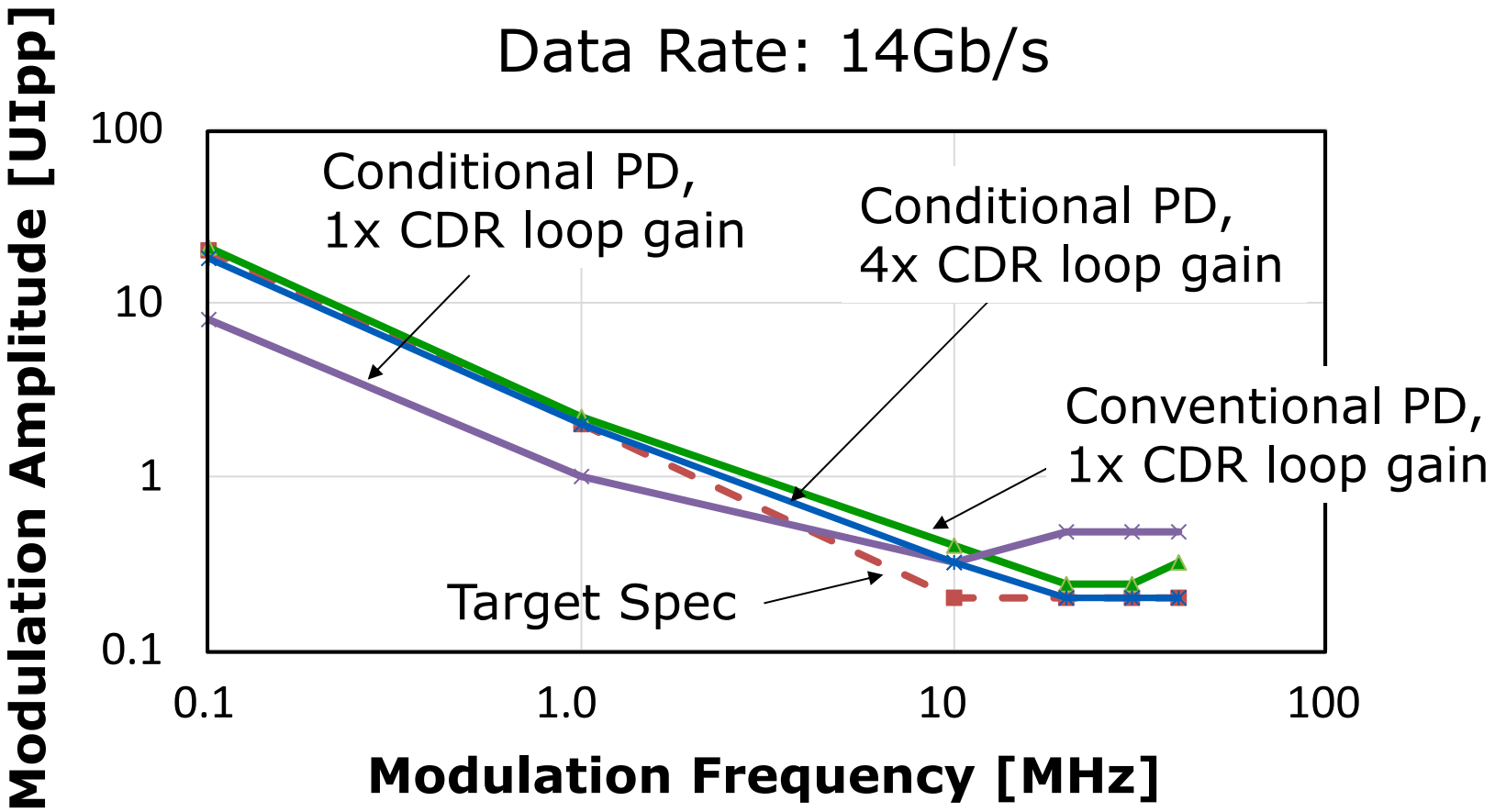
(PLL power not included)

Measured Power Efficiency



(PLL power not included)

Jitter Tolerance Measurements



- Conditional PD meets target specification

Comparison Table

	[1]	[2]	[6]	This work	
CMOS technology	32nm	28nm	32nm	22nm	
Supply voltage		0.9V	0.95V	0.9V	1.07V
Data rate [Gb/s]	28	32	11.8	16	32
Channel loss at Nyquist	35dB	40dB	25dB	24dB	16dB
TX FFE	4-tap	3-tap	3-tap	3-tap	
RX DFE	15-tap	2-tap	4-tap	6-tap	
RX peaking amplifier	2-stage	2-stage	1-stage	1-stage	
Transceiver power efficiency per lane (pJ/b)	24.8*	7.5 (RX only)	6.6**	4.6*	6.4*

* PLL power amortized over 4 lanes

** PLL power amortized over 8 lanes

Summary

- Power-performance scalable
  - 4Gb/s to 32Gb/s
  - 1pJ/b to 5.7pJ/b
- Bundle TX/RX clock
- Bidirectional transceiver
- Dual-mode RX front-end
- Conditional CDR
- Cable and low-profile connector

Acknowledgement

We would like to thank the following individuals for their valuable contributions:

V. Baca, K. Aygun, A. Zhang, P. Parmar, M. Balasubramanian, S. Thakare, A. Kornfeld, D. Duarte, P. Stolt, W.-H. Wang, T. Chan-Carusone, C. Thakkar, S. Spangler, Y. Fan, A. Mezhiba, M. Haycock, Y. Ling, H. Heck, D. Ackelson, M. Bell and S. Spina

A Pin and Power Efficient Low Latency 8-12Gb/s/wire 8b8w-Coded SerDes Link for High Loss Channels in 40nm Technology

Anant Singh[1], Dario Carnelli[1] , Altay Falay[1], Klaas Hofstra[1], Fabio Licciardello[1], Kia Salimi[1], Hugo Santos[1], Amin Shokrollahi[1], Roger Ulrich[1], Christoph Walter[1], John Fox[2], Peter Hunt[2], John Keay[2], Richard Simpson[2], Andy Stewart[2], Giuseppe Surace[2], Harm Cronie[3]

[1]Kandou Bus, Lausanne, Switzerland,
[2]Kandou Bus, Northampton, United Kingdom,
[3]Lausanne, Switzerland

Outline

- Introduction and motivation
- Macro architecture
  - TX
  - RX
- System Implementation
- Results
- Conclusion

Motivation

- Demand for semiconductor component IO data bandwidth is increasing, pin count is not: need to transmit more bits per pin per second
- Many industries expect doubling the throughput at equal (or lower) power at every generation
- Traditional methods are running out of steam.

Throughput Increase

- Change the channel (expensive)
- Change the signaling (cost depends)
  - One direction: multi-level (4-PAM, 8-PAM, etc)

Throughput Increase

- Change the channel (expensive)
- Change the signaling (cost depends)
  - One direction: multi-level (4-PAM, 8-PAM, etc)
  - Another direction: Pool more than two wires together, and disperse information among them
    - Generalization of differential signaling

Chord Signaling

- We have developed a whole new theory of signaling based on information dispersal among multiple wires to increase throughput, reduce power, and combat noise
- Theory has similarities to MIMO in wireless systems, but is unique to chip-to-chip communication

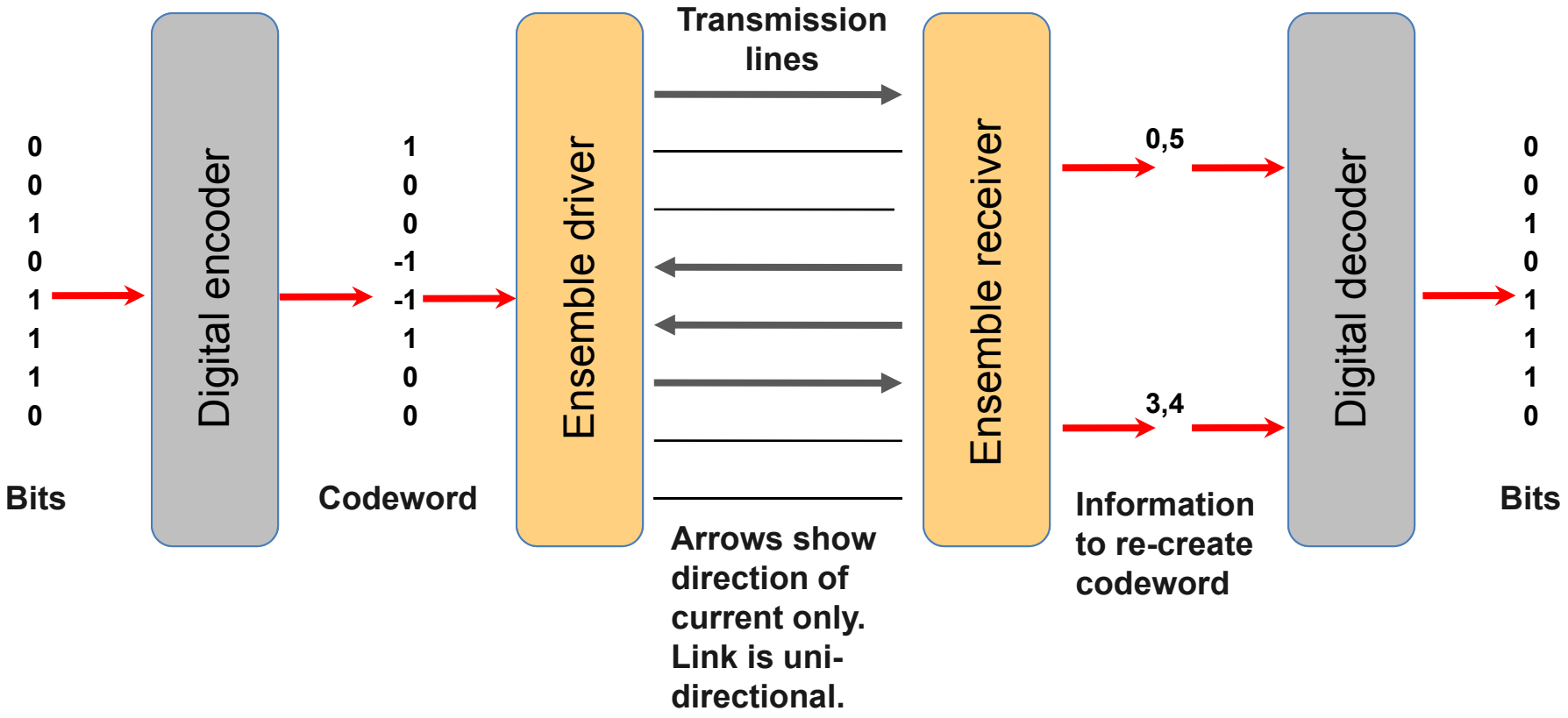
This Talk

- Report on implementation of one of the chord signaling methods, called 8b8w
- 8 bits of information are dispersed among 8 wires
- Pin-efficiency of single-ended signaling, but much better signal integrity through differential type receivers
- Only one instantiation of a general technique.

8b8w Coding

- At every UI
  - two of the eight wires are driven high (+1),
  - two are driven low (-1),
  - and four are left at common mode (0).
- Information is encoded in the positions of the high/low/quiet wires

Conceptual View



Codebook

- Total number of distinct permutations of (+1,+1,0,0,0,0,-1,-1) is

$$\frac{8!}{2! \times 2! \times 4!} = 420$$

- Of these 256 are chosen judiciously to minimize encoding/decoding complexity
- 8 bits are transmitted per UI.

Quiescent Communication

- Codeword is uniquely determined by the positions of the 0's and +1's
  - The 0's don't use active power
  - But their positions count for 6 of the 8 bits
- 6 of the 8 bits are communicated via quiescence, without using active line power.
- Line power is that of two differential pairs, throughput is 4 times as large.

8b8w-Coded SerDes Link

- Transmits 8-bits over an 8-wire interface
  - Pin efficiency is 1
- Differential legacy mode transmits 4-bits on the same 8-wire interface (as 4 differential pairs)
  - Pin efficiency is 0.5

Encoder

- Implements the codebook efficiently

Encoder

- Implements the codebook efficiently
  - No table look-up

8b8w Codebook

- Implements a codebook efficiently
  - No table look-up

Code Properties

- If (c_1,.., c_8) is a codeword produced by encoder, then current (voltage) of strength c_1 is applied to the first wire, current (voltage) c_2 is applied to the second wire, etc
- $c_1 + \ldots + c_8 = 0$
  - Zero common mode and SSO noise
- Receiver uses reference-less comparator network to determine codeword

Outline

- Introduction
- Macro Architecture
  - TX
  - RX
- System Implementation
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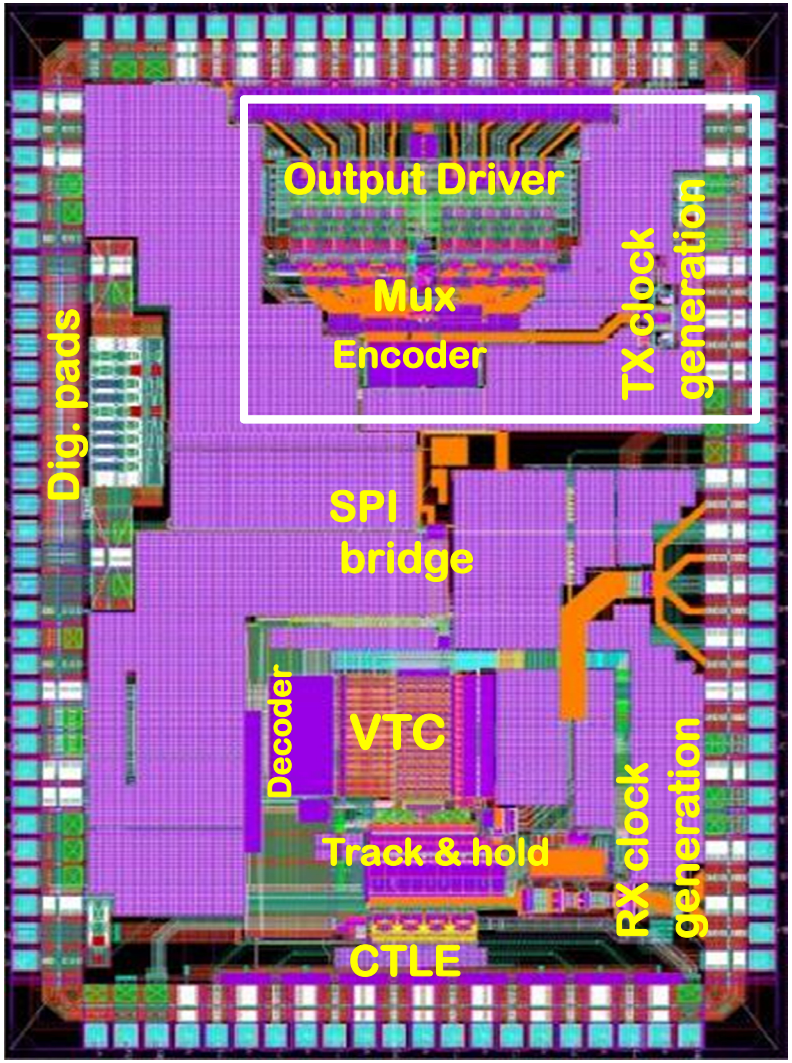
Macro Architecture

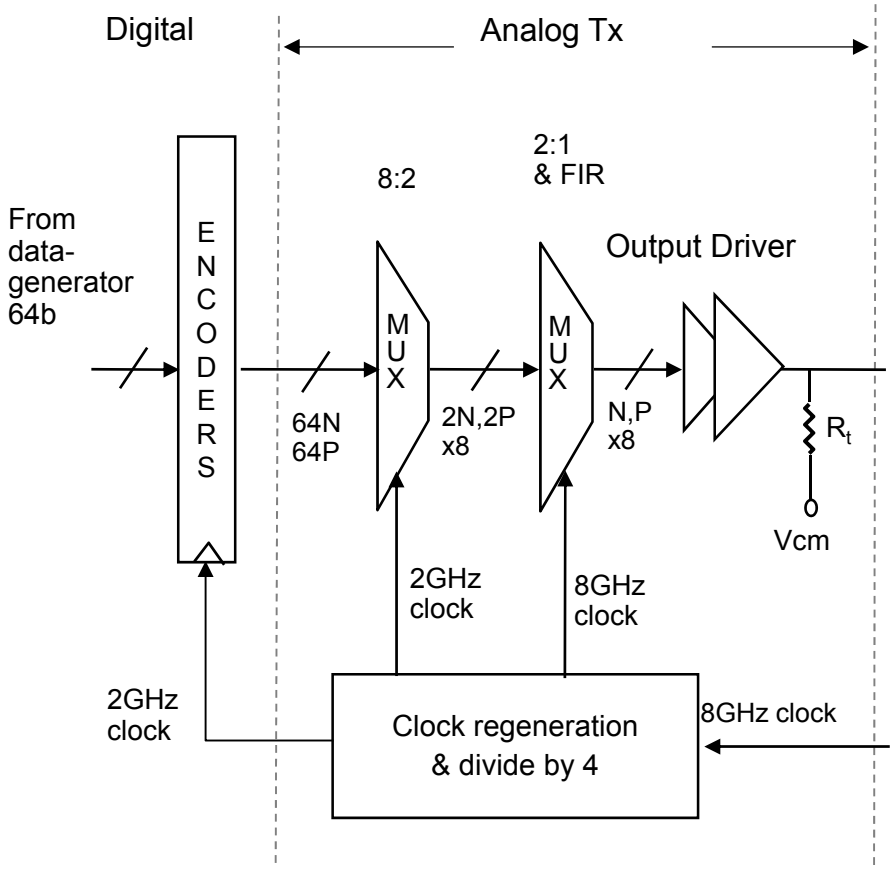
- Components:
  - TX
    - Pattern generators, encoder, serializer
    - Output Driver, FIR
  - RX
    - CTLE, multi-phase detector & sampled system, decoder, error-checkers
    - Eye scope
  - Clock generation
  - Chip control
  - Differential legacy mode is included for comparison and testing



3mm x 2mm

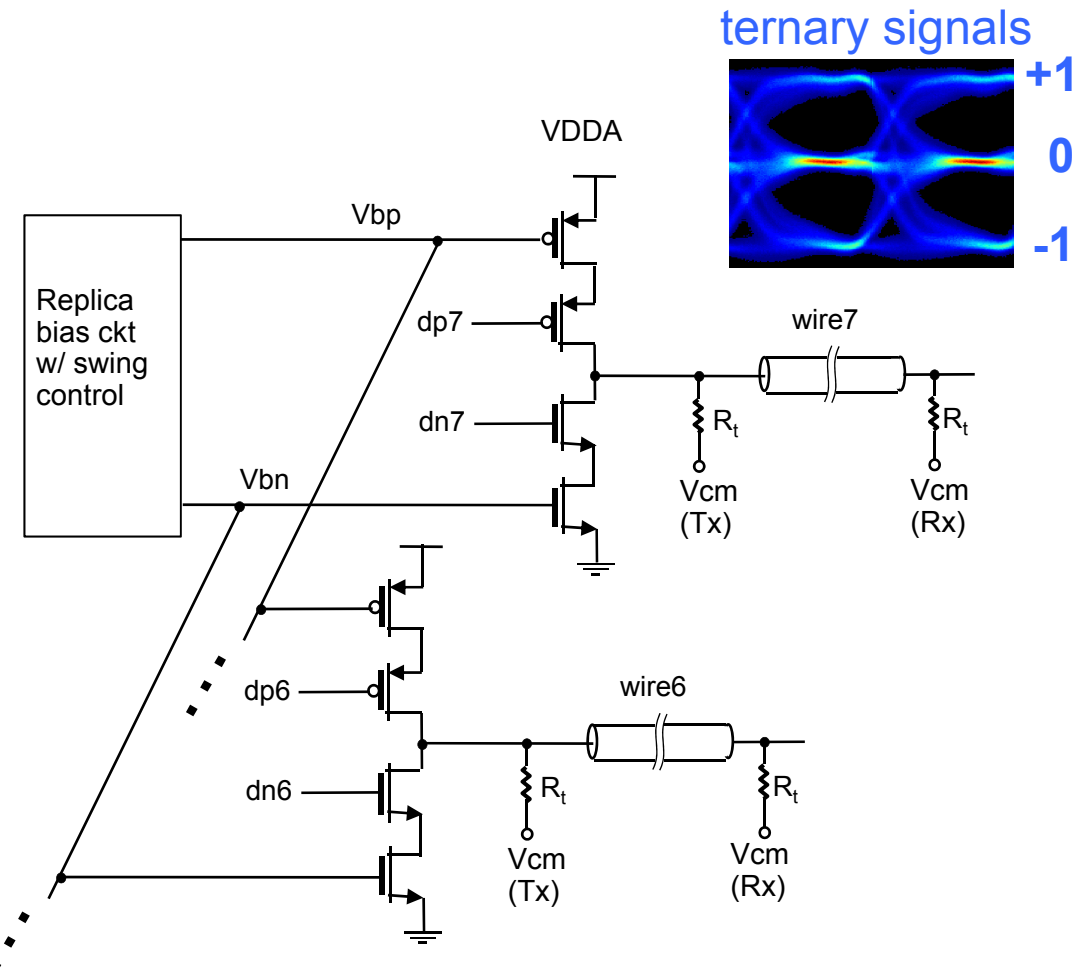
Transmitter

- Digital encoder
- 8:1 serializer



Output Driver

- Current mode
- 2-tap FIR



Macro Architecture

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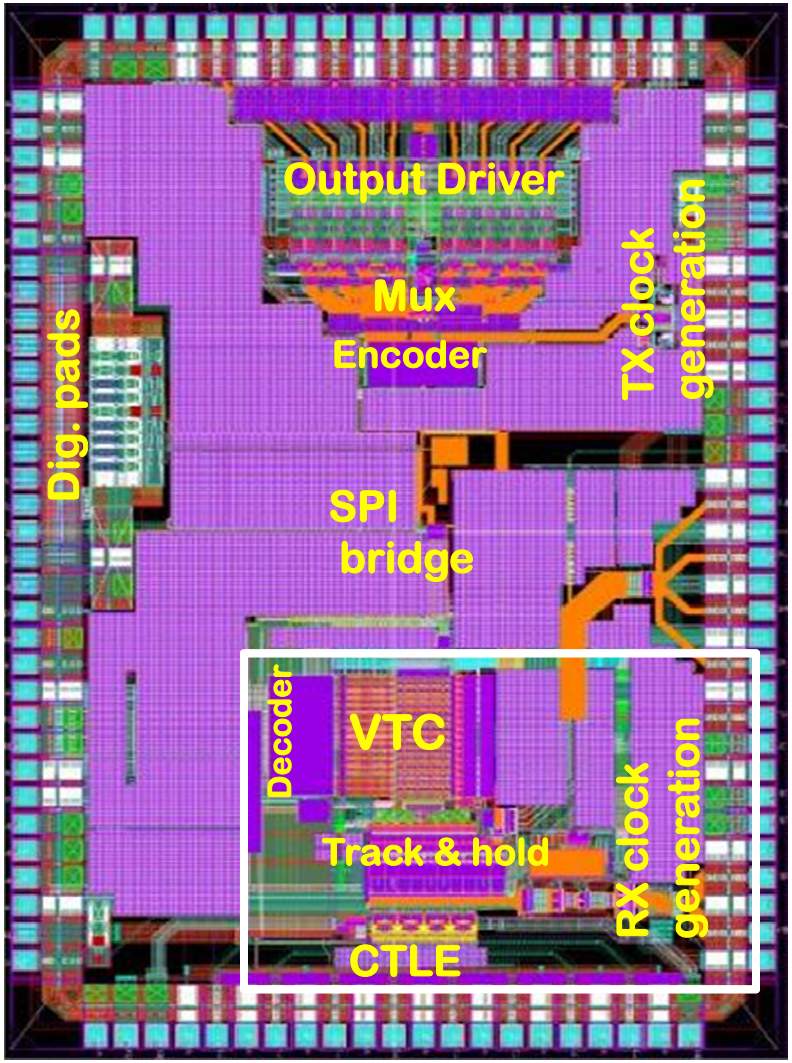
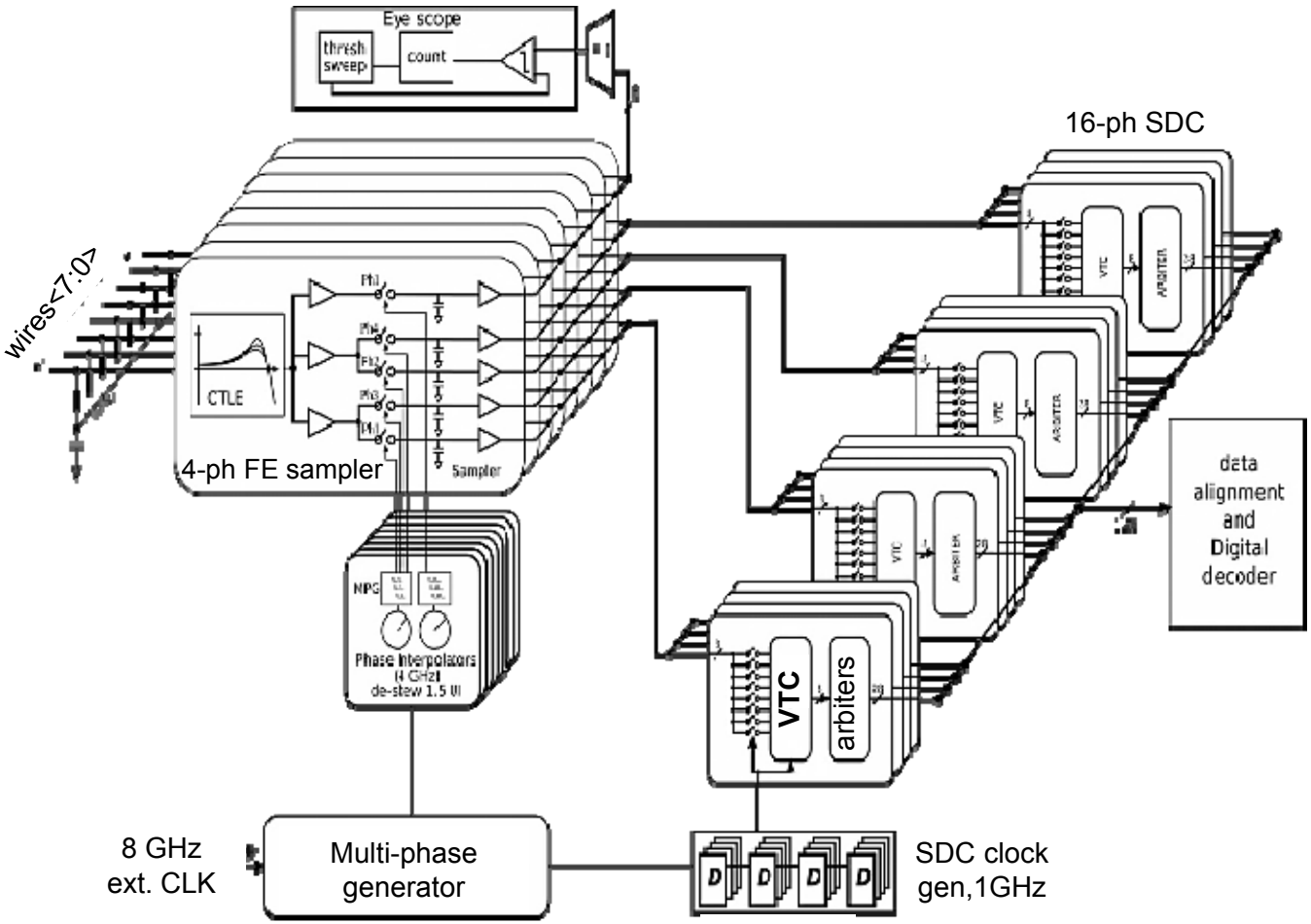


3mm x 2mm

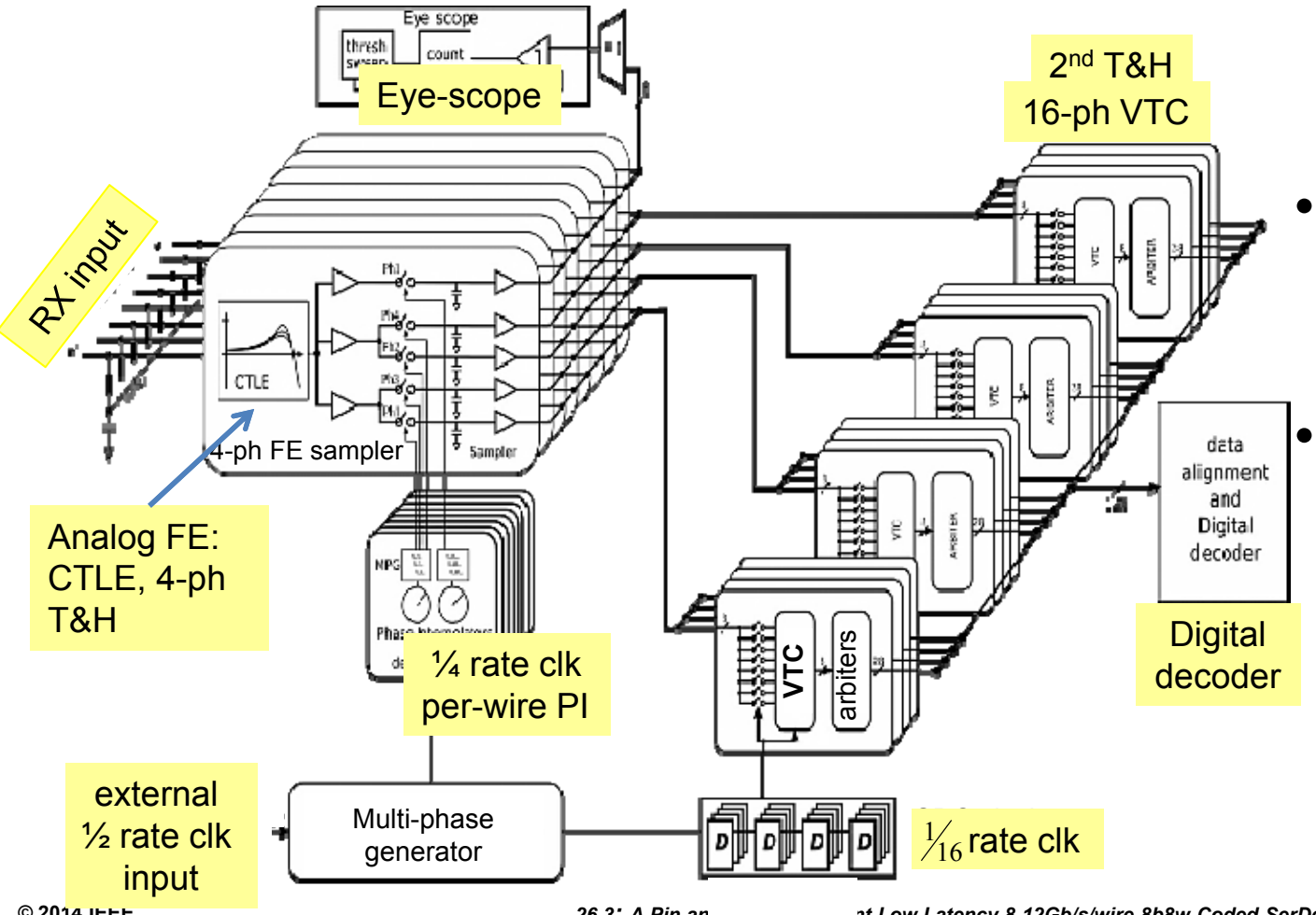
Receiver

- Analog front end rank-orders the wires based on detected voltage levels
- Digital logic detects positions of two maxima (‘+1’s) and two minima (‘-1’s) in order to decode the bits
- Information is encoded in the positions, not the actual values on the wires
- Our receiver actually completely rank orders the wire values

Receiver Top Level



Receiver Top Level



- 16-phase time interleaved system
- ½ rate external clock used as input
- Per-wire phase interpolators (PI) produce ¼ rate sampling clocks

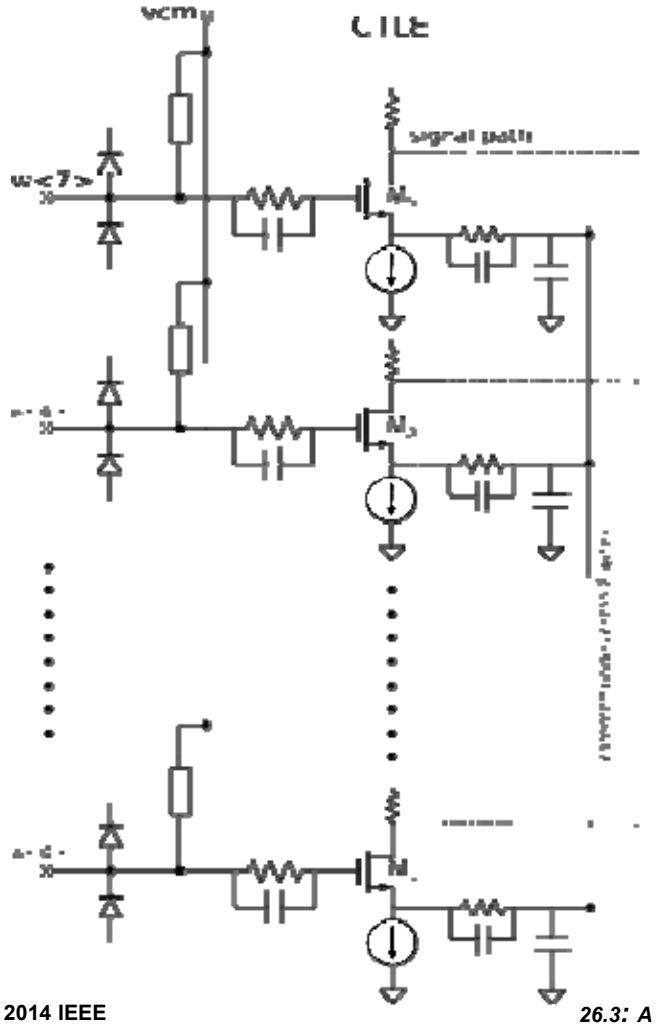
Analog Front End

- Designed to pass high frequency common mode signal in order to allow realignment (de-skew) without distortion

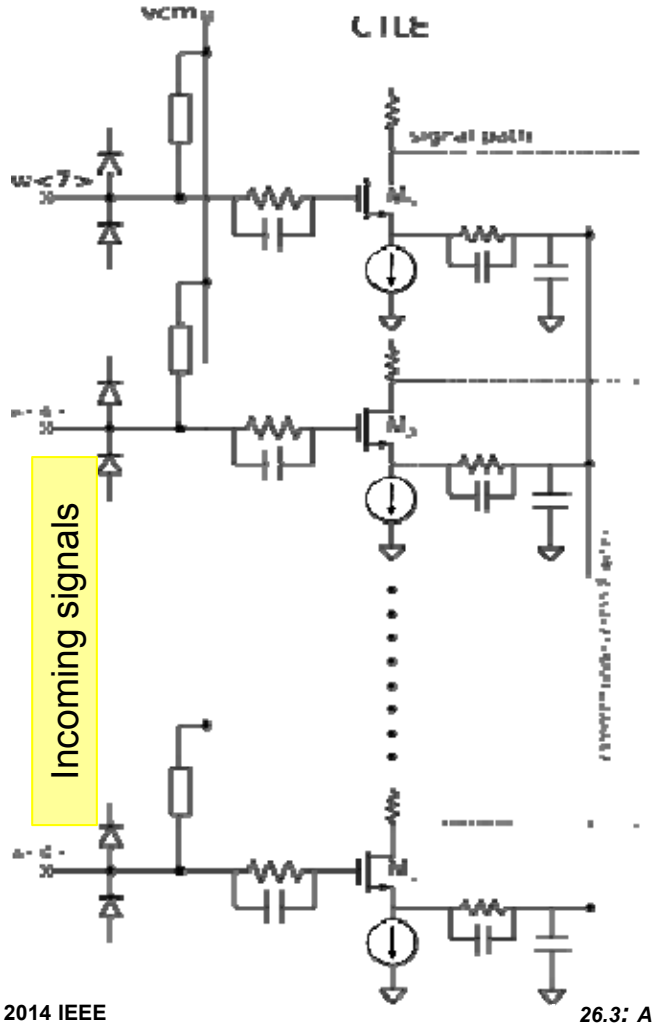
Analog Front End

- Designed to pass high frequency common mode signal in order to allow realignment (de-skew) without distortion
- Suppresses low frequency common mode noise

Analog Front End

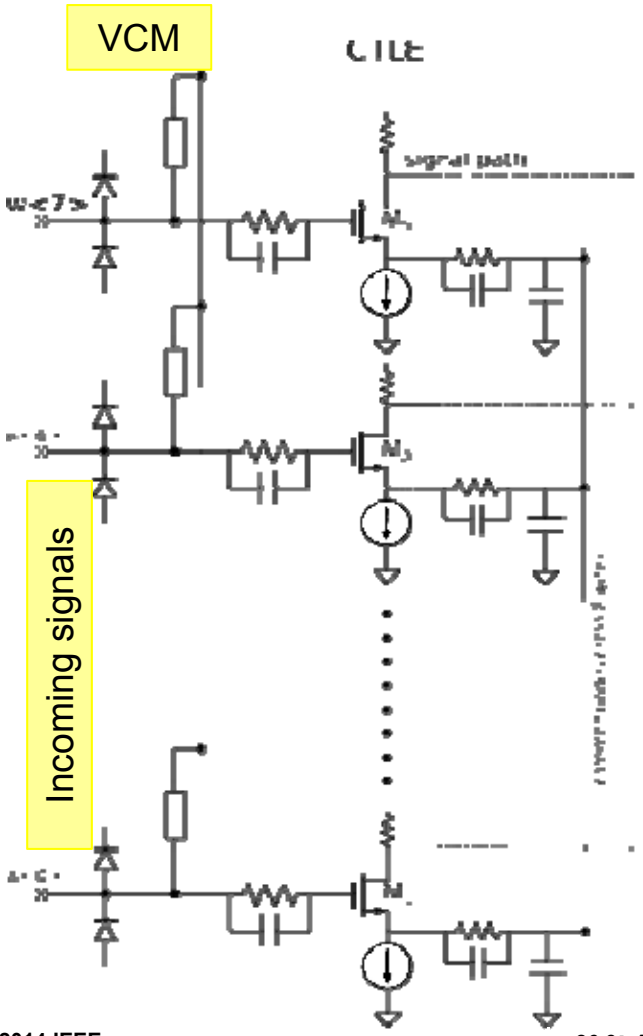


Analog Front End



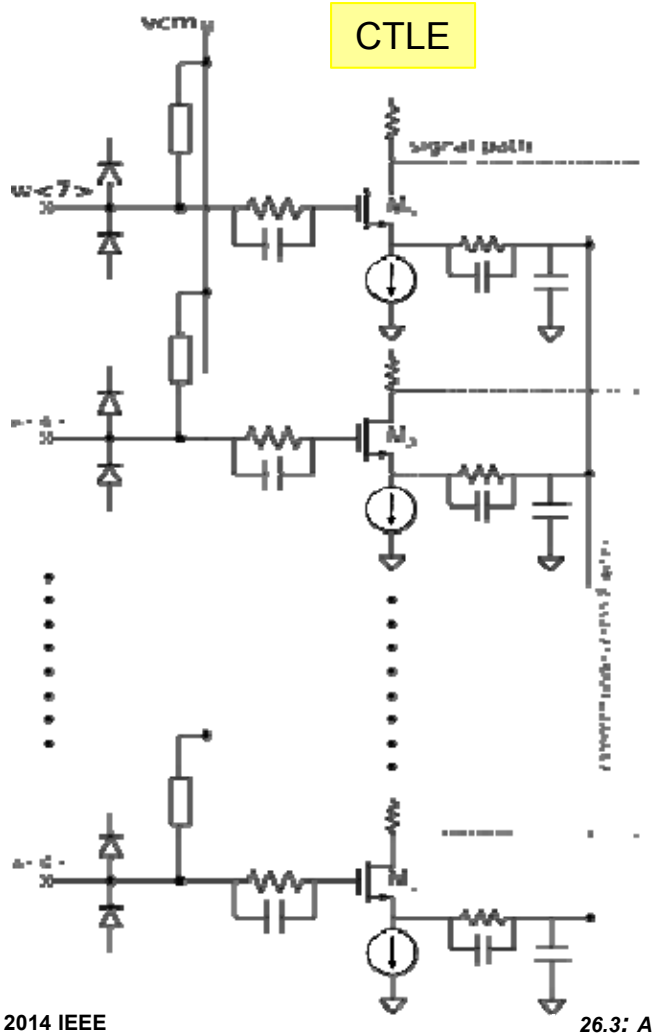
– Input is DC coupled

Analog Front End



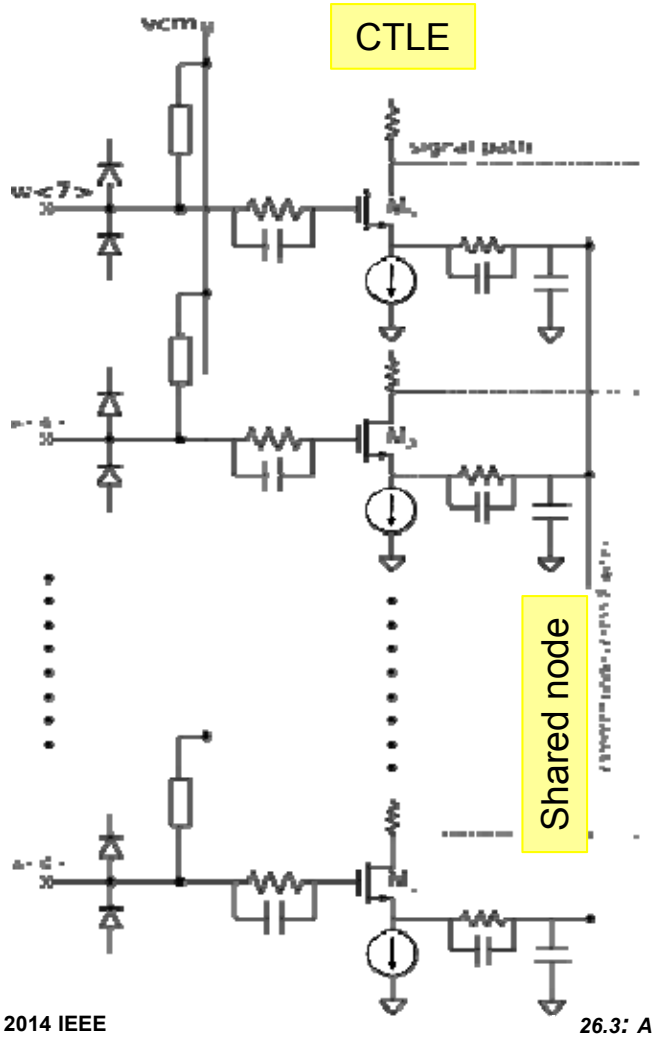
- Input is DC coupled
- Level shifter sets the appropriate common mode for the input stage

Analog Front End



– CTLE
  - Hybrid between a generalized differential pair and a common-source amplifier

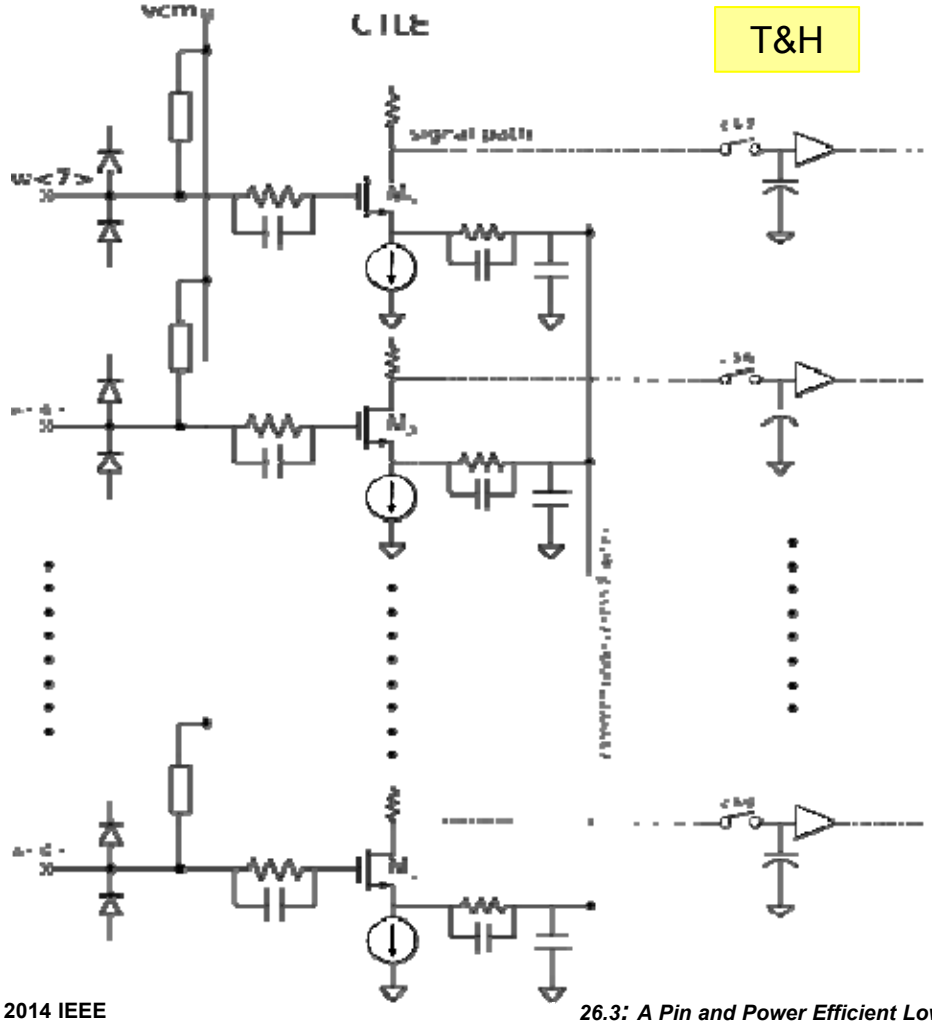
Analog Front End



– CTLE

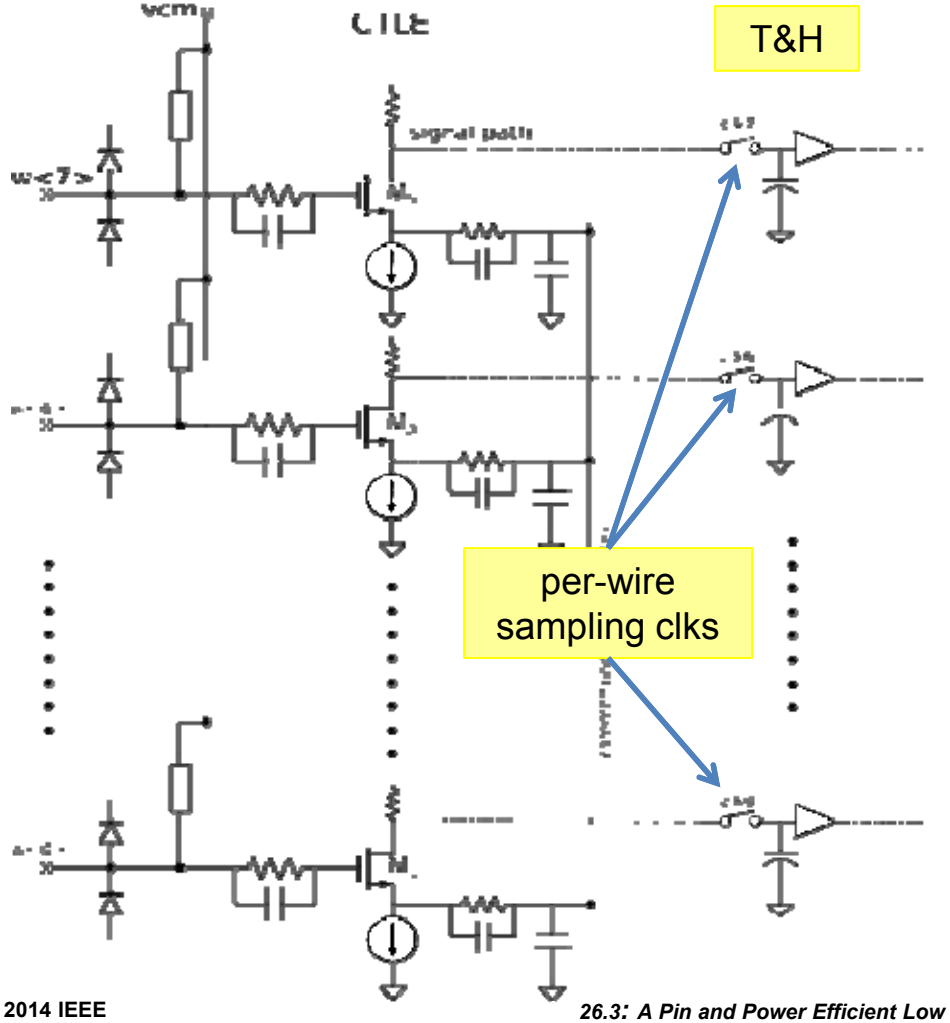
- Hybrid between a generalized differential pair and a common-source amplifier
- The shared node is stabilized at high frequencies by capacitors effectively turning the structure into a single-ended common-source amplifier with source degeneration

Signal Path



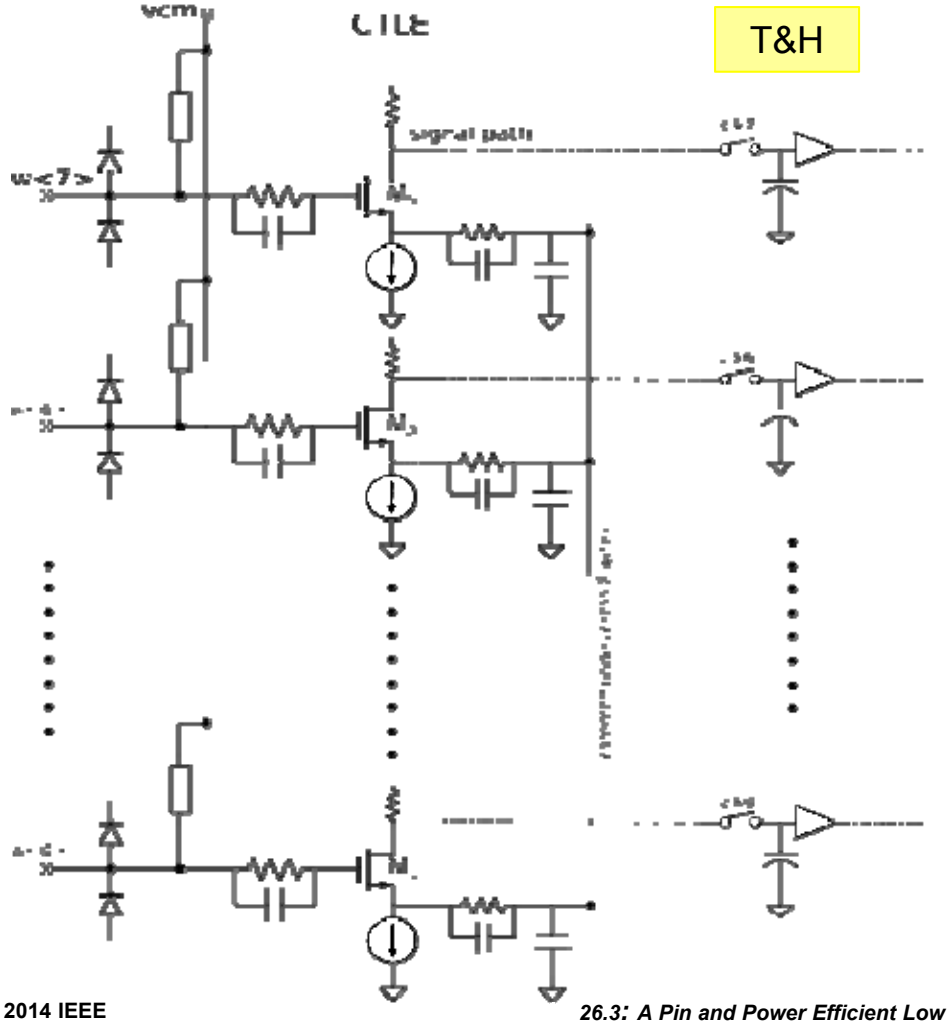
– CTLE is followed by track and hold circuits (T&H)

Signal Path



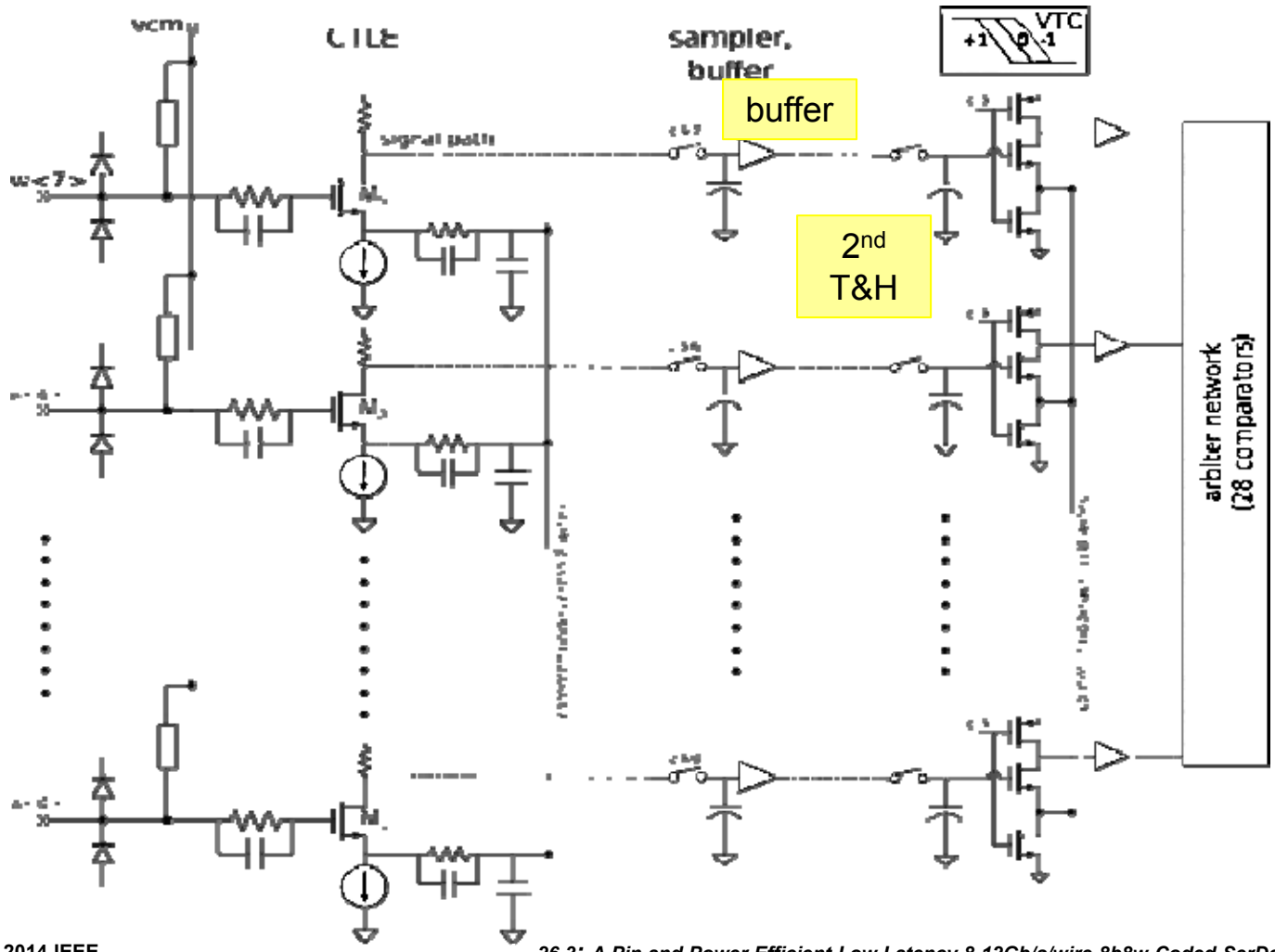
- CTLE is followed by track and hold circuits (T&H)
- Sampling clocks can be adjusted per-wire for de-skewing the incoming signals up to 1UI

Signal Path



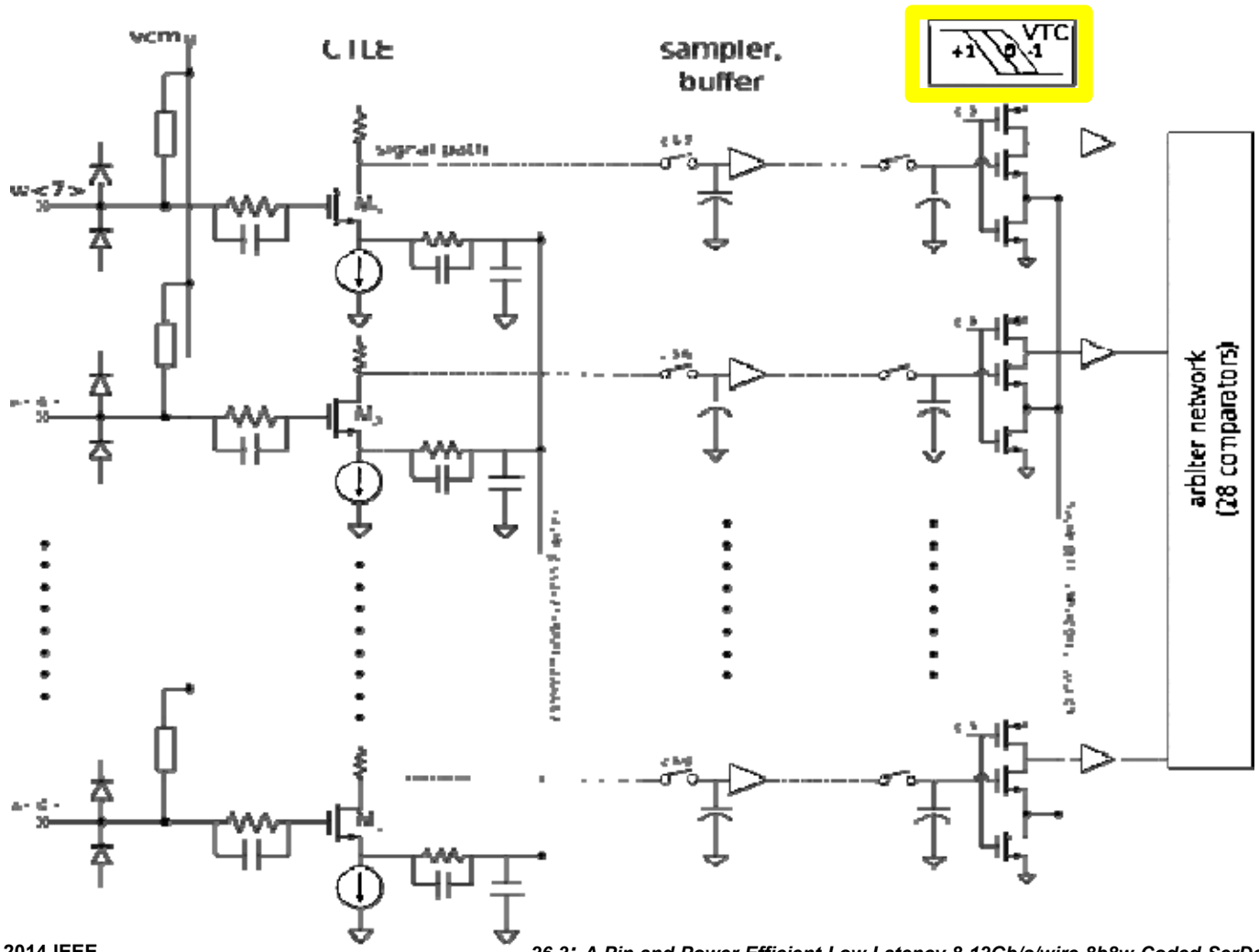
- CTLE is followed by track and hold circuits (T&H)
- Sampling clocks can be adjusted per-wire for de-skewing the incoming signals up to 1UI
- T&H operates at 1/4th rate (4-phase system)

Signal Path



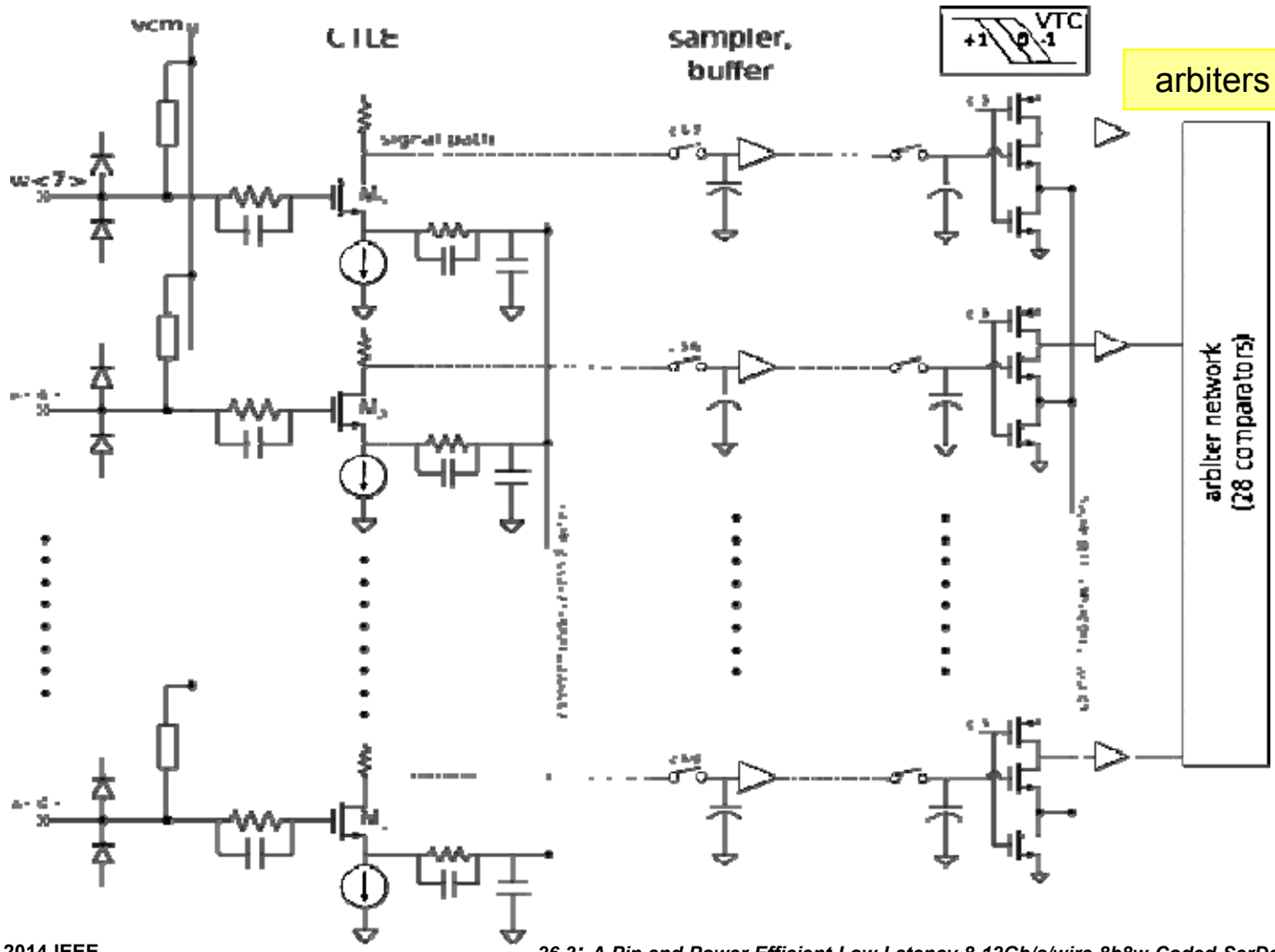
– Buffer drives aligned signals to 2nd T&H circuit (operates at 1/16th rate)

Signal Path



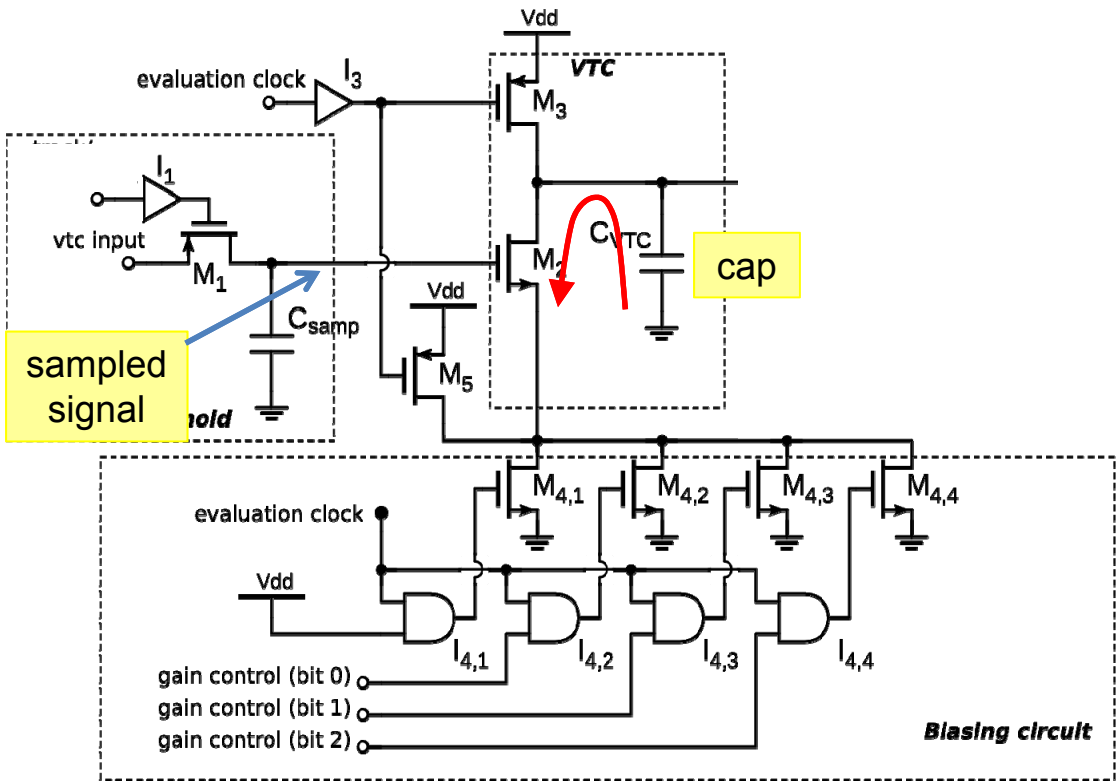
- Buffer drives aligned signals to 2nd T&H circuit (operates at 1/16th rate)
- VTC produces an edge at time proportional to sampled voltage

Signal Path



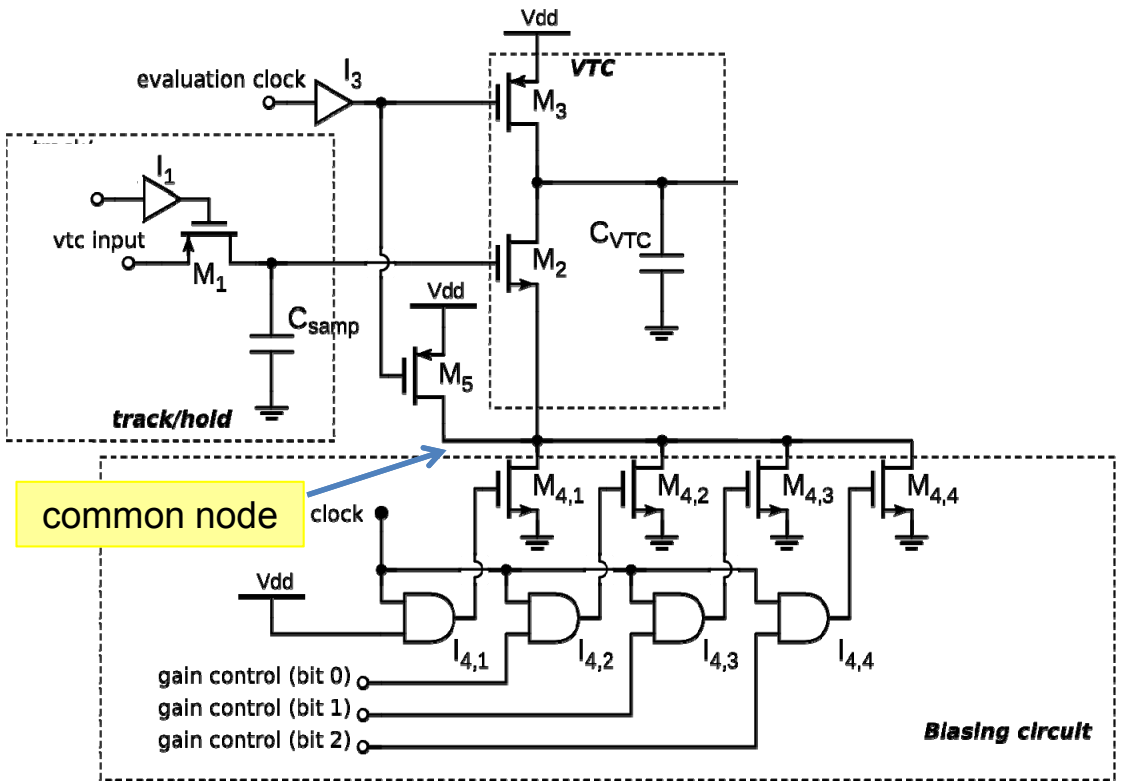
- Buffer drives aligned signals to 2nd T&H circuit (operates at 1/16th rate)
- VTC produces an edge at time proportional to sampled voltage
- Arbiter network compares the arrival times of edges to rank order the wires

VTC



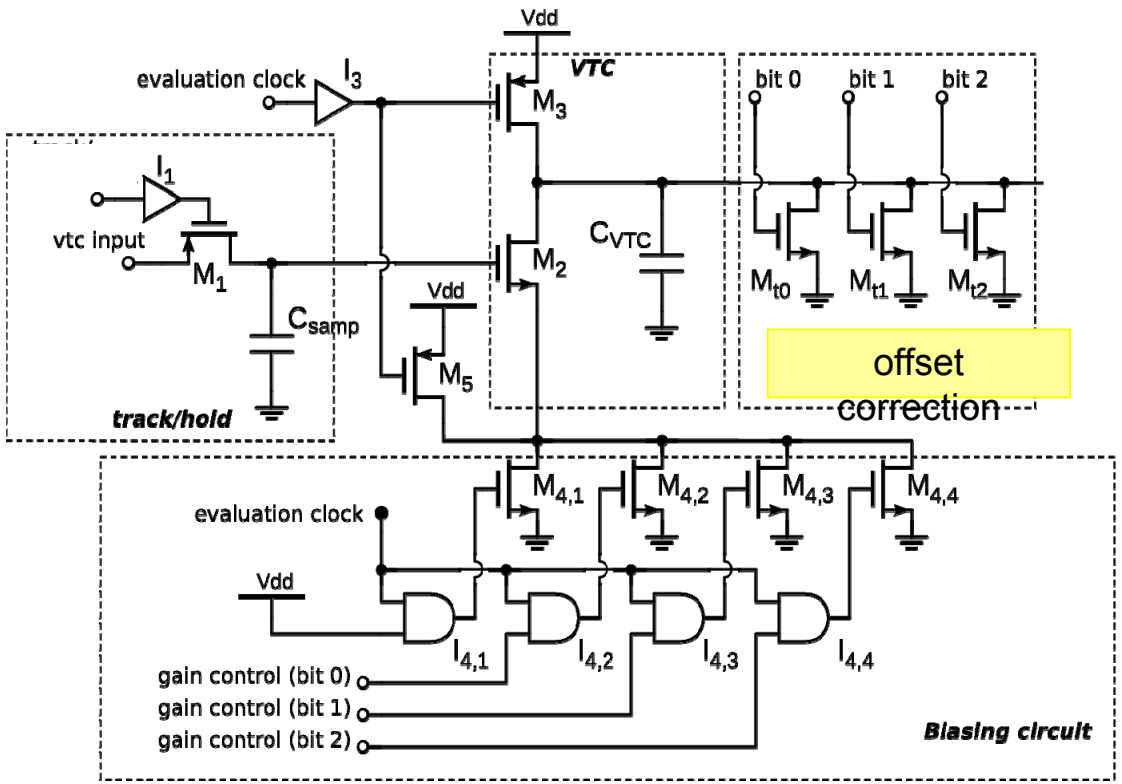
– Converts the sampled voltage to a ramp by discharging a pre-charged capacitor

VTC



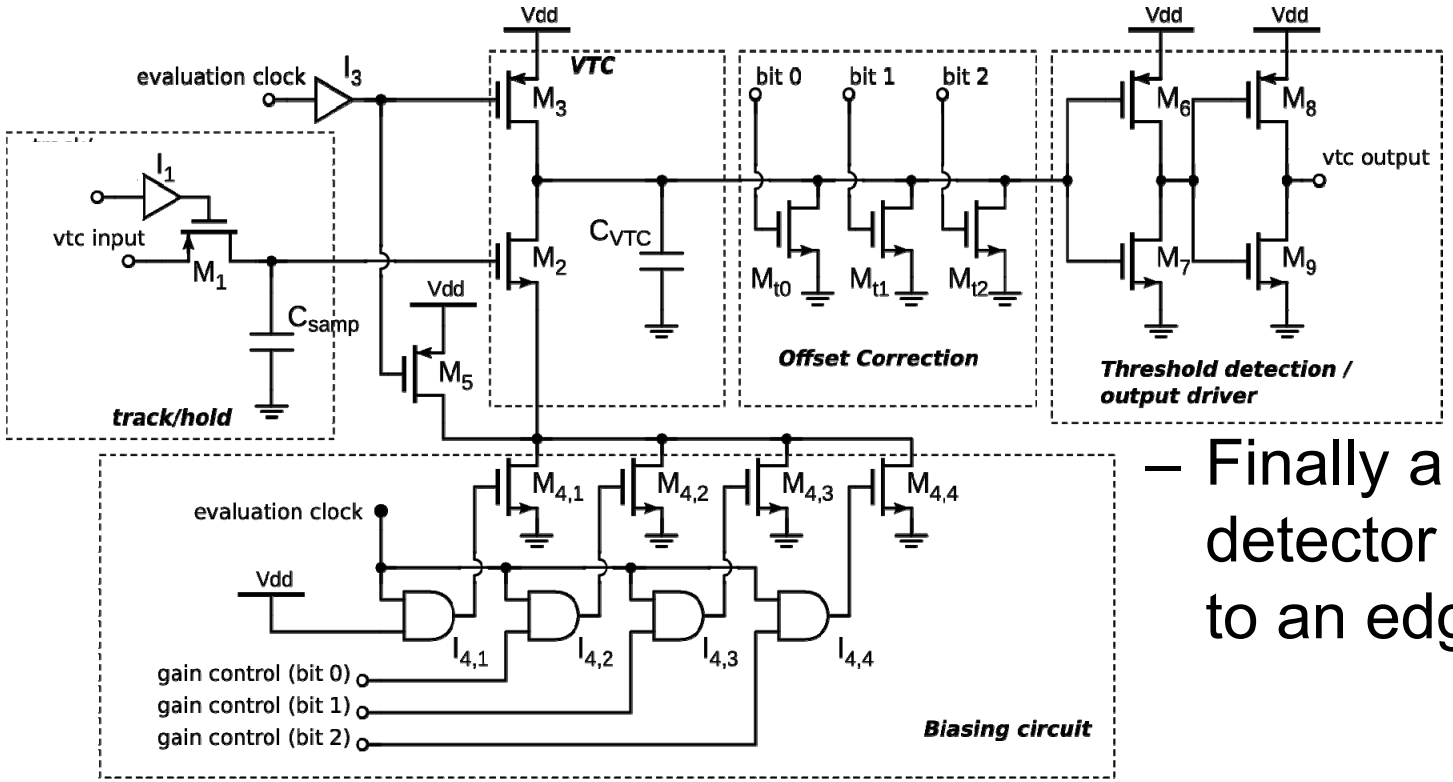
- Converts the sampled voltage to a ramp by discharging a pre-charged capacitor
- Has controlled current source with common tail device across the 8 wires, which allows for different gain settings

VTC



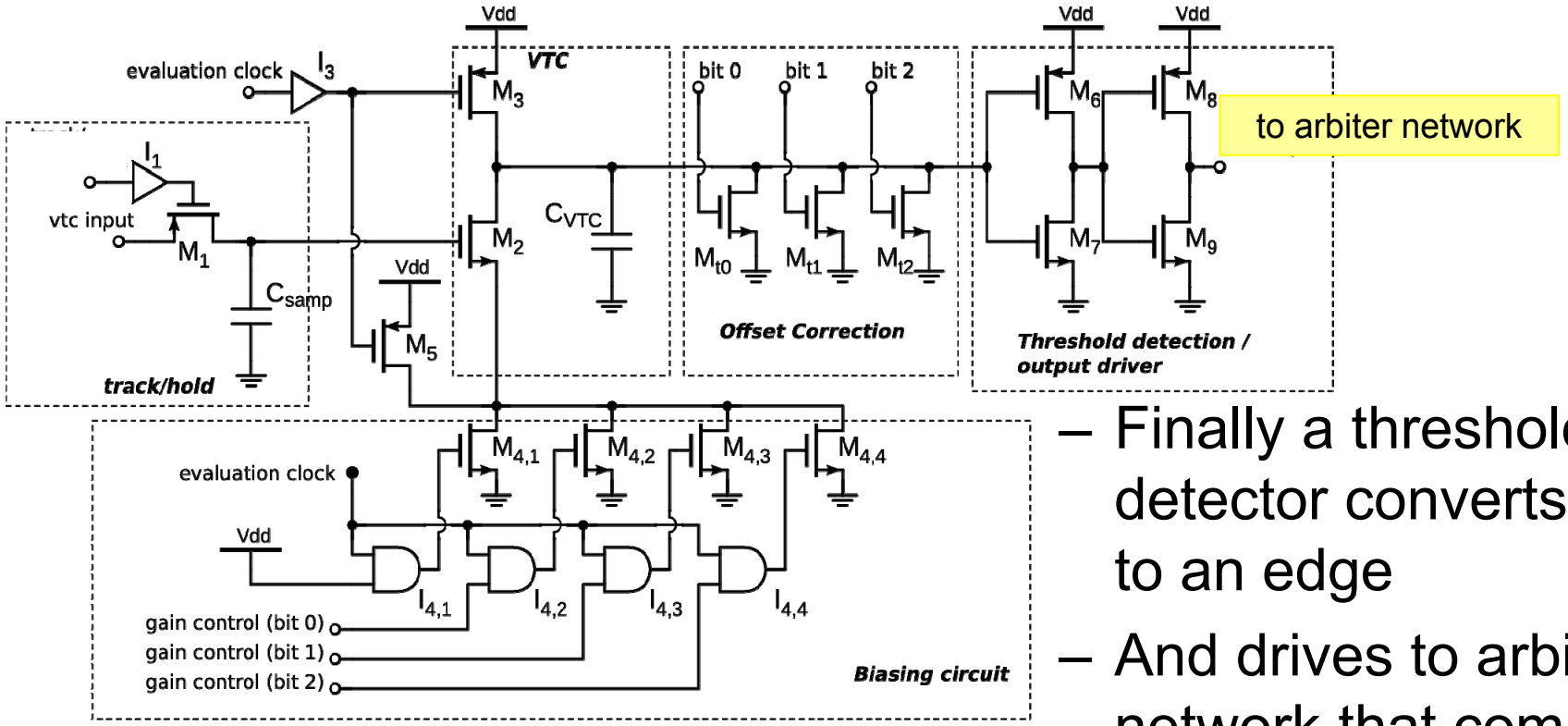
- Converts the sampled voltage to a ramp by discharging a pre-charged capacitor
- Has controlled current source with common tail device across the 8 wires, which allows for different gain settings
- Includes offset correction

VTC



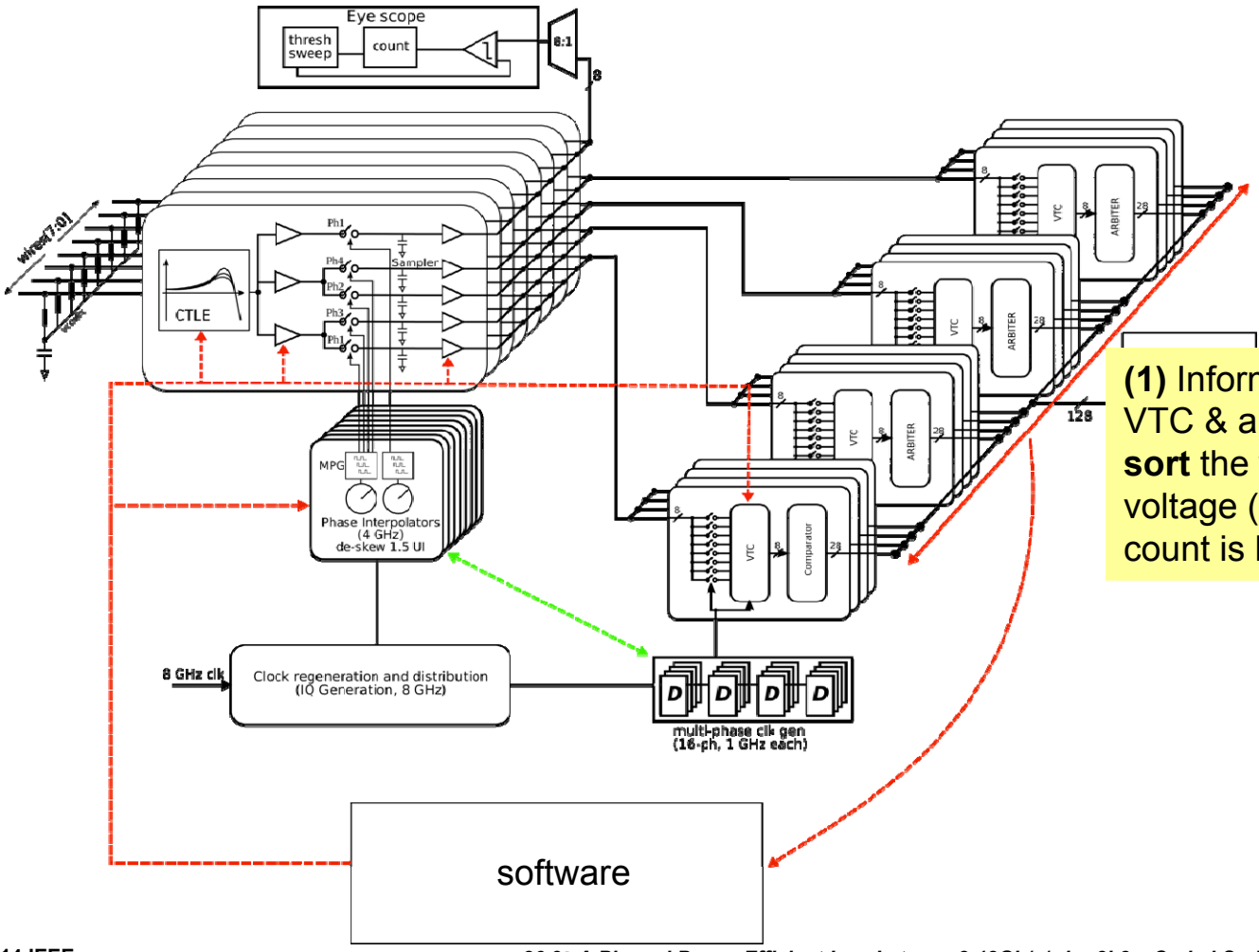
– Finally a threshold detector converts ramp to an edge

VTC



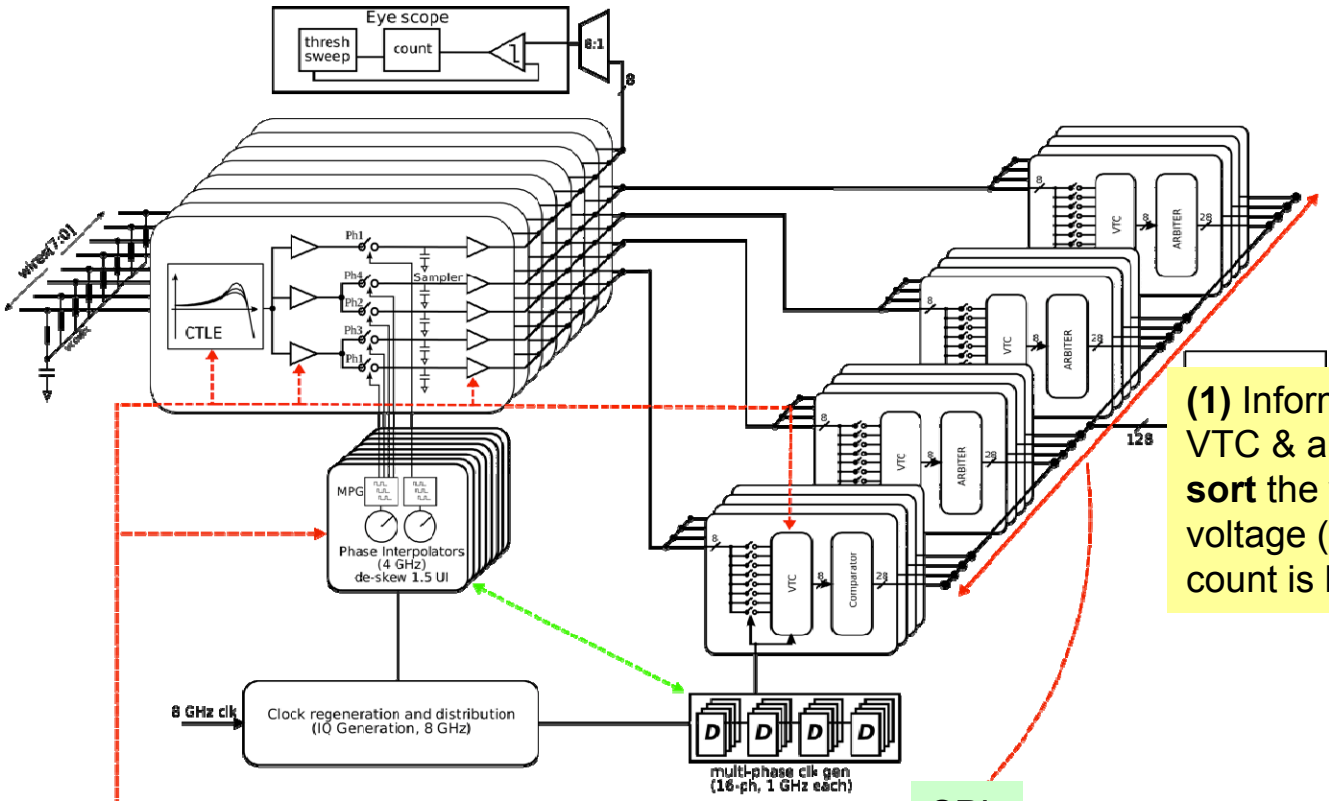
- Finally a threshold detector converts ramp to an edge
- And drives to arbiter network that compares arrival times of the 8 edges

Receiver Control Loops



(1) Information is used from VTC & arbiter network to **sort** the wires based on voltage (max to min). Error count is logged

Receiver Control Loops

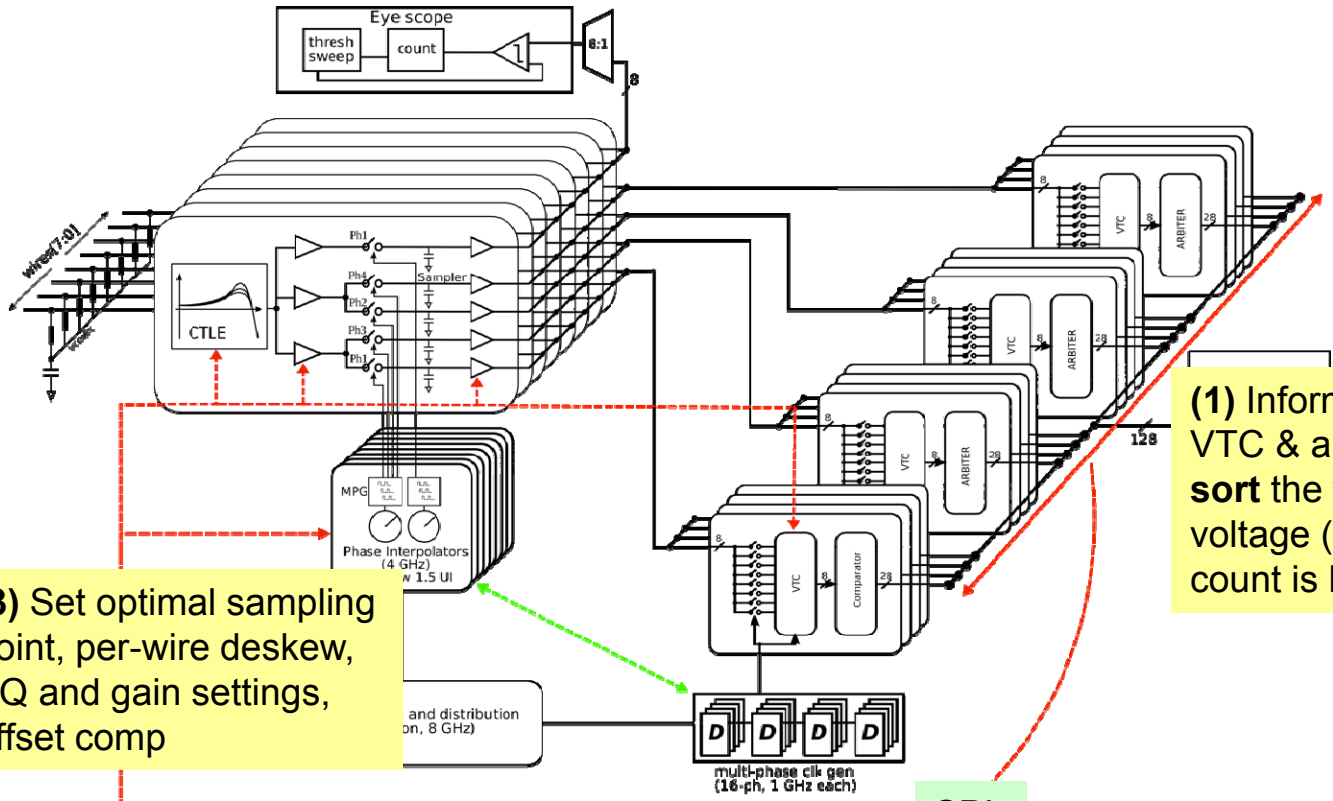


(1) Information is used from VTC & arbiter network to **sort** the wires based on voltage (max to min). Error count is logged

SPI

(2) Code aware algorithms run in software that use sorting info for timing optimization

Receiver Control Loops



(1) Information is used from VTC & arbiter network to **sort** the wires based on voltage (max to min). Error count is logged

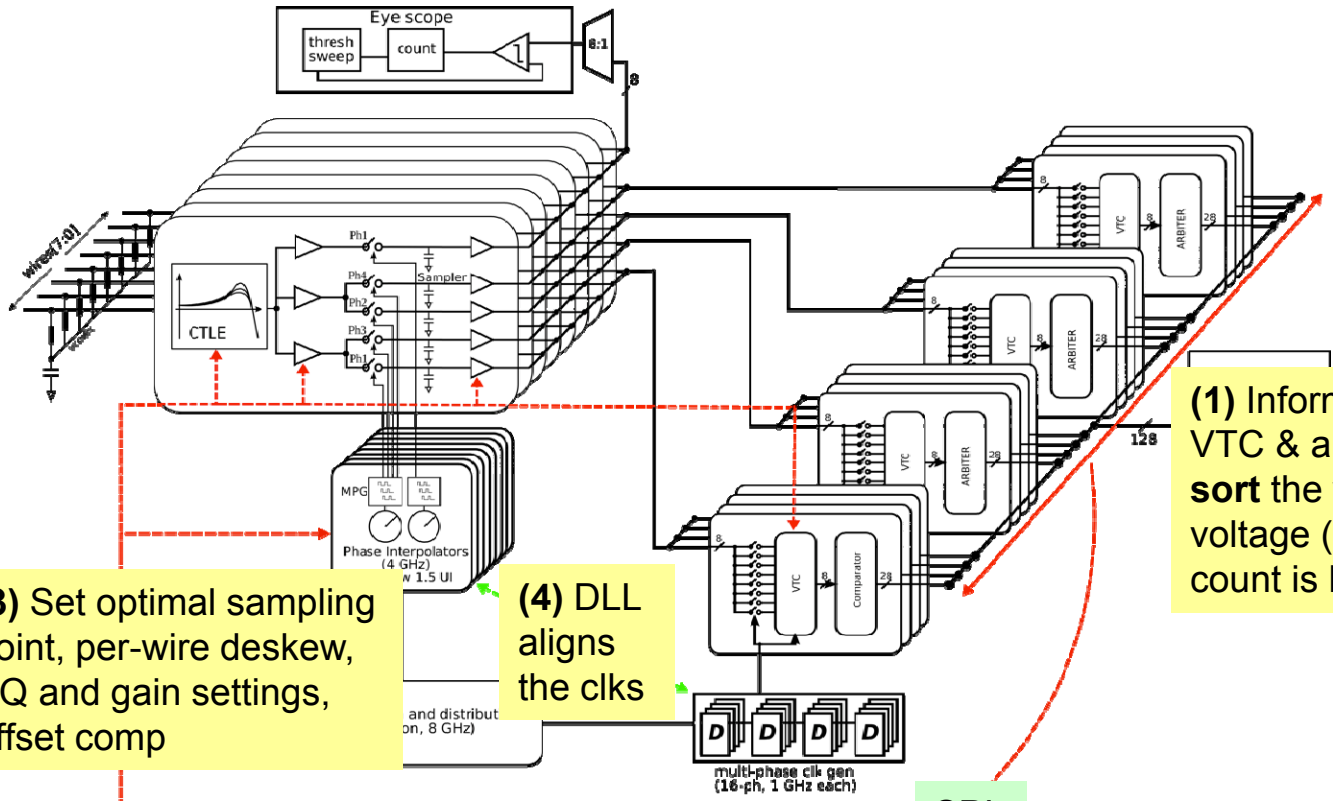
(3) Set optimal sampling point, per-wire deskew, EQ and gain settings, offset comp

SPI

(2) Code aware algorithms run in software that use sorting info for timing optimization

SPI

Receiver Control Loops



(1) Information is used from VTC & arbiter network to **sort** the wires based on voltage (max to min). Error count is logged

(3) Set optimal sampling point, per-wire deskew, EQ and gain settings, offset comp

(4) DLL aligns the clks

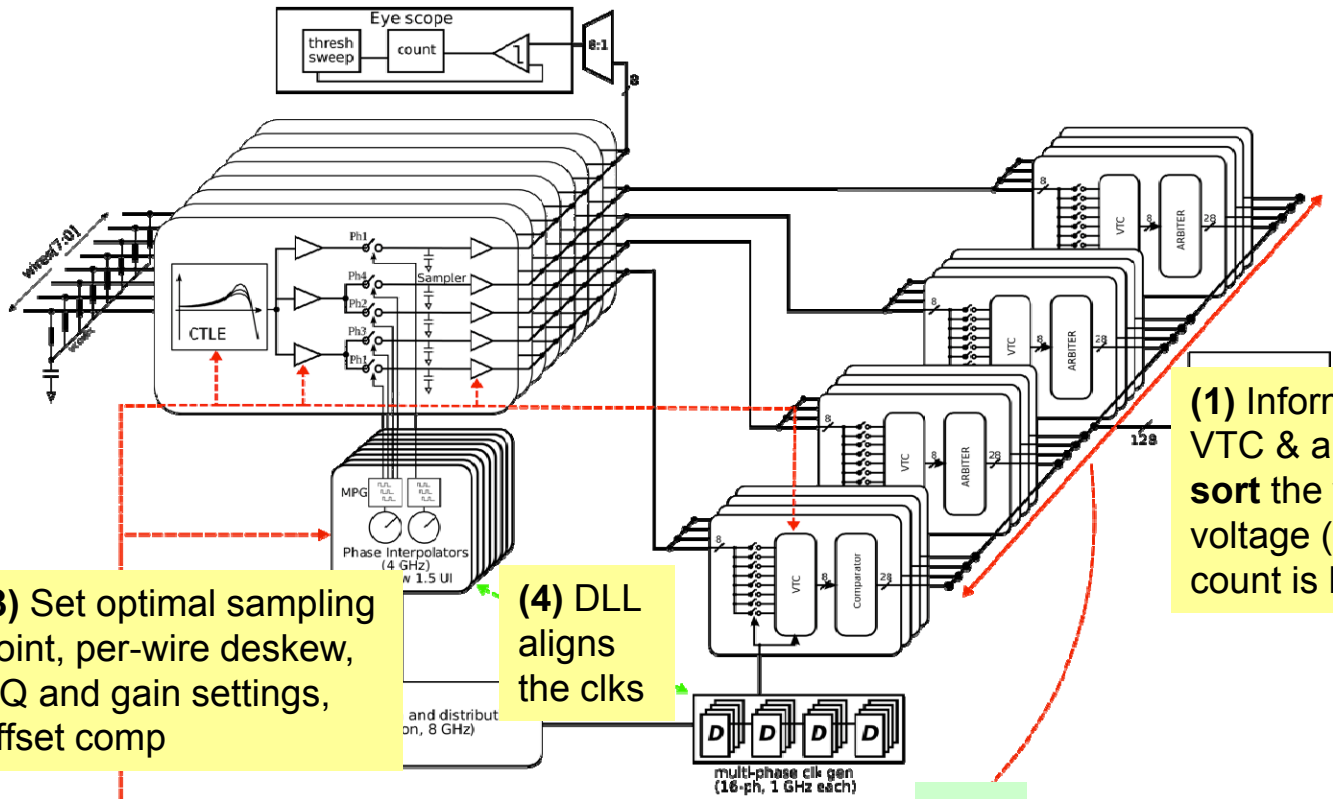
SPI

(2) Code aware algorithms run in software that use sorting info for timing optimization

SPI

Receiver Control Loops

– Control loops run continuously and adapt to incoming signal



(1) Information is used from VTC & arbiter network to **sort** the wires based on voltage (max to min). Error count is logged

(3) Set optimal sampling point, per-wire deskew, EQ and gain settings, offset comp

(4) DLL aligns the clks

SPI

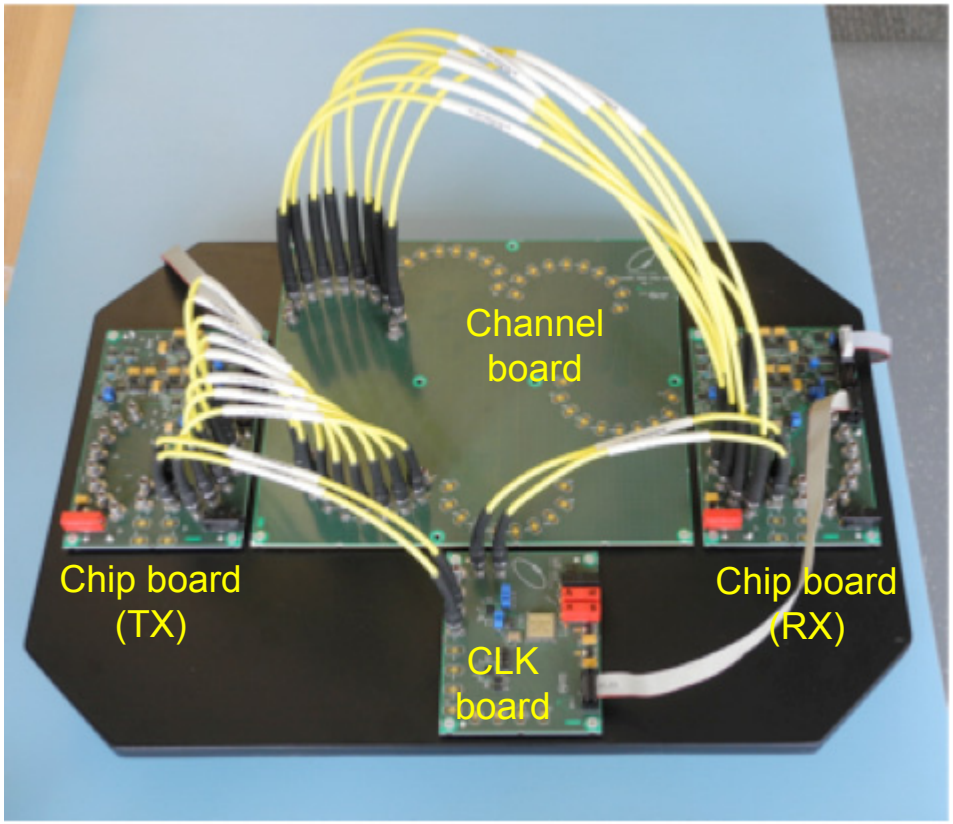
(2) Code aware algorithms run in software that use sorting info for timing optimization

SPI

Outline

- Introduction
- Macro Architecture
  - TX
  - RX
- System Implementation
- Results
- Conclusion

System Implementation

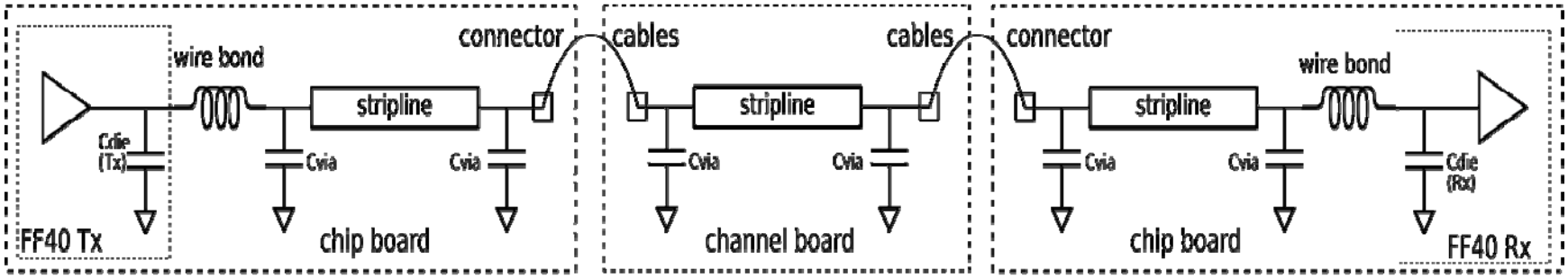


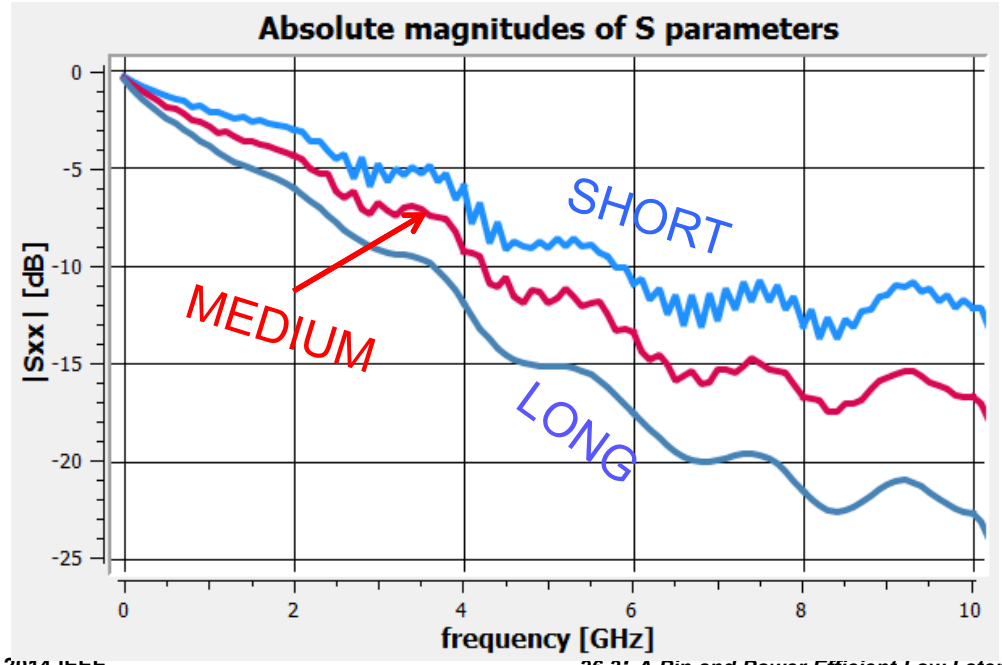
Industrial Demo Session on Monday, Feb 10th, 2014

- **DUT**
  - Chip board with transceiver mounted as chip-on-board, I/O fan-out to 2x8 SMA connectors, SPI test interface, DAC-controlled power supplies
- **Channel:**
  - Channel board with 3 sets of traces, for a total channel length of 369mm/556mm/792mm (Rogers RO4350B/RO4450F), IL 12-17dB
- **Clock:**
  - Custom clock PCB generating 4-8GHz differential clocks

System Implementation

- Test system and channel

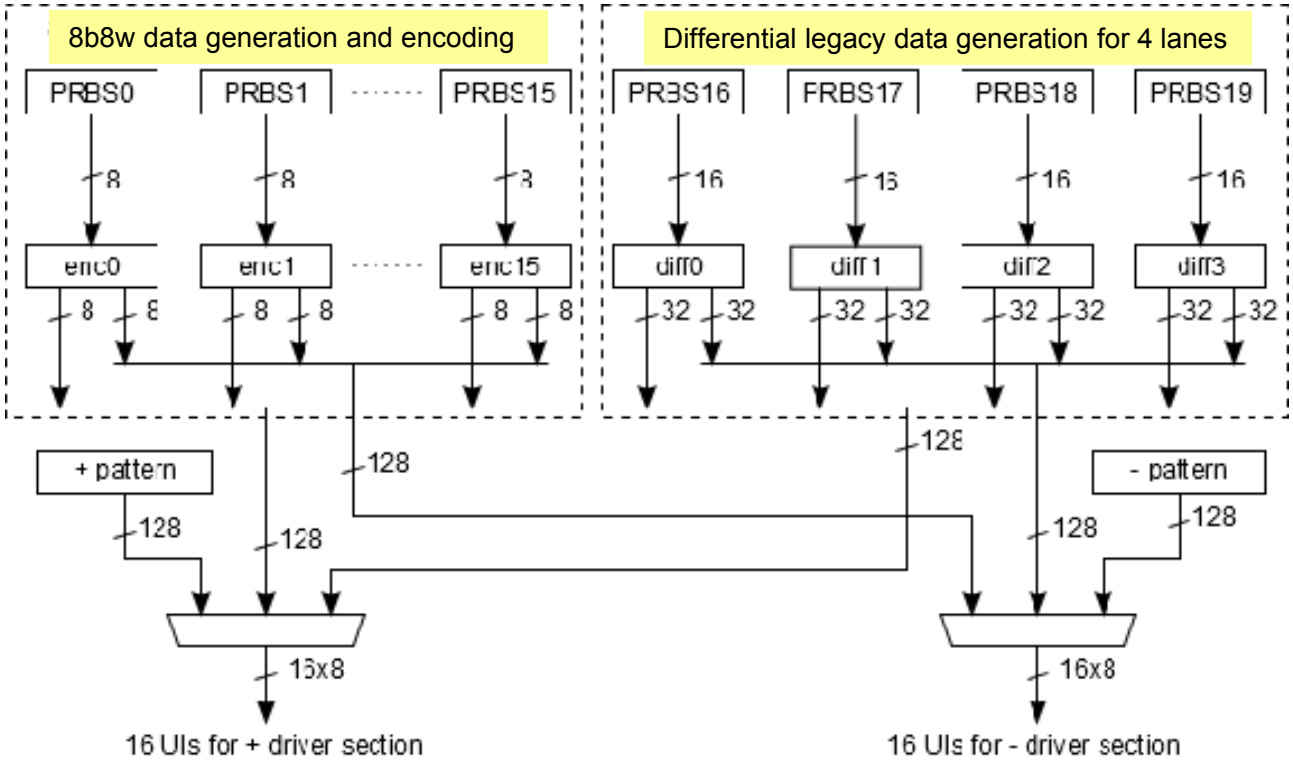




- Channel losses
  - Channel board IL is in the range of 12-17dB at 6GHz
  - Additional 5dB loss due to chip board traces, connectors and cables
  - Wire bond inductance is in the range of 1-1.5nH

System Implementation

- Data generators and test patterns



– Modes:
  - 8b8w
  - Differential (legacy)
– Patterns
  - PRBS9
  - PRBS31
  - Custom

Outline

- Introduction
- Macro Architecture
  - TX
  - RX
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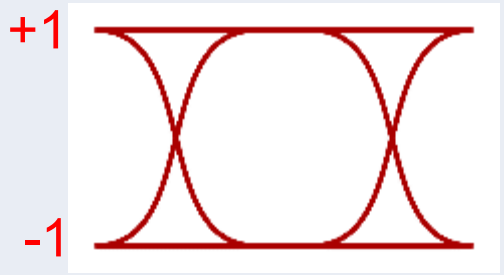
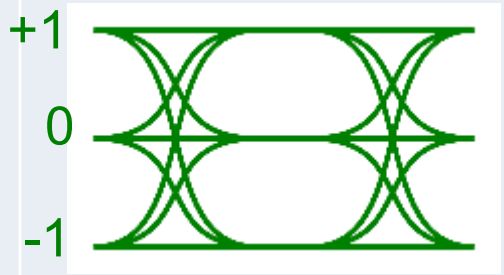
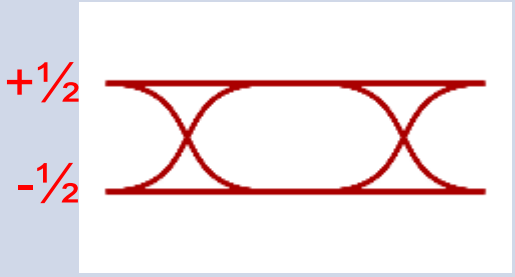
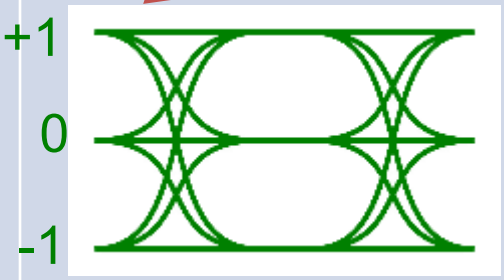
8b8w vs Differential

	Differential signaling	8b8w signaling
Reference-less receiver	YES	YES
Balanced signals	YES	YES
Wires required for 8 bits	**16**	**8**
Line power for 8 bit, equal peak-to-peak	8 	2 
Line power for 8 bit, equal noise margin	**4** 	**2** 

Results

- Differential mode vs. 8b8w mode

GBaud	Differential Mode		8b8w Mode	
	Gb/s/ wire	Gb/s (8-wires)	Gb/s/ wire	Gb/s (8-wires)
8	4	32	8	64
12	6	48	12	96
16	8	64	16	128

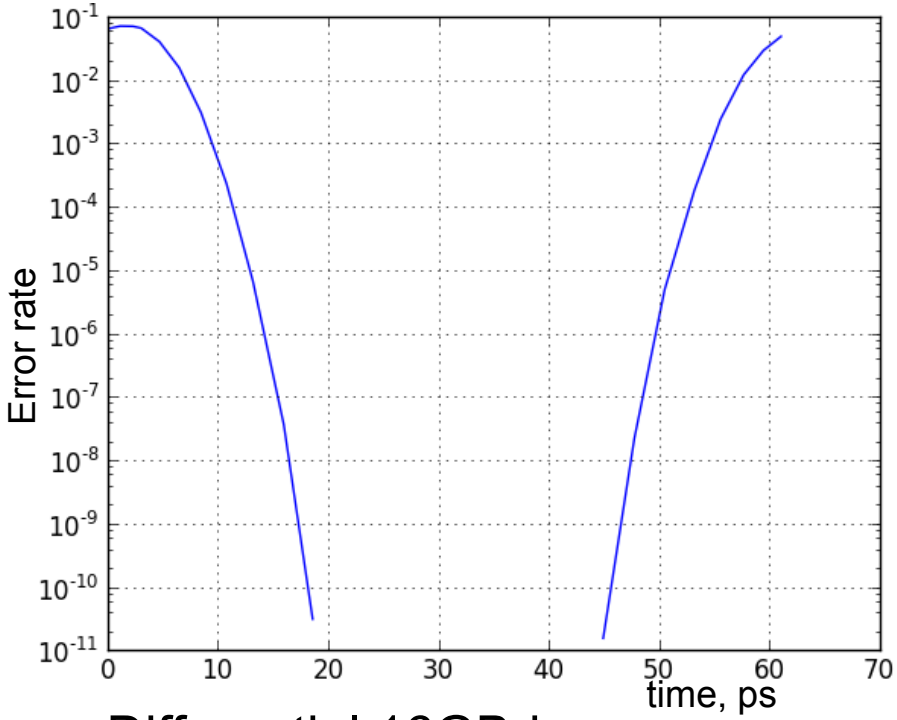
- Legacy differential-pair mode needs to run at 16Gbd vs. 8b8w mode at 8Gbd in order to deliver the same effective throughput (64Gb/s)

	Differential Mode **@16Gbd**	8b8w Mode **@8Gbd**
Total,mW	504.53	316.61
pJ/bit	**7.88**	**4.95**

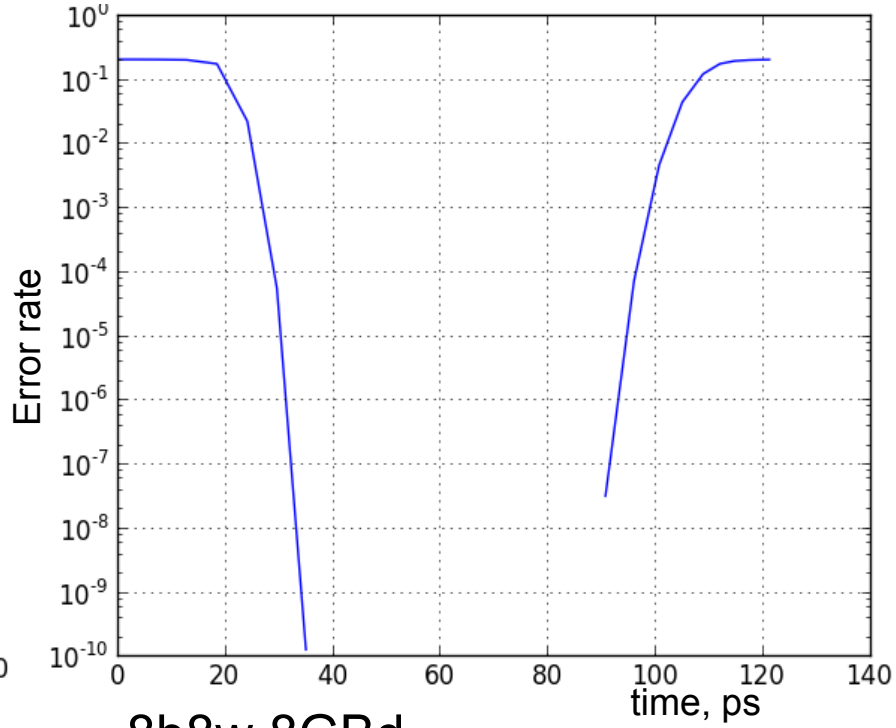
- Measured power consumption is about 40% lower at same effective throughput

Results

- Differential mode vs. 8b8w mode:
  - Measured bathtub plots at equivalent throughput (64Gb/s)



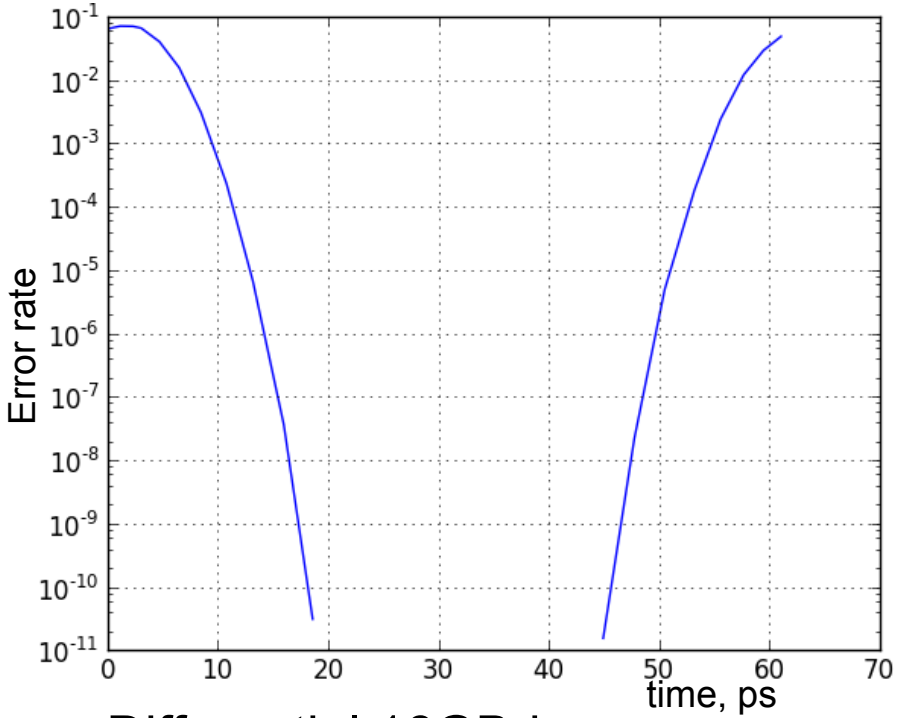
Differential 16GBd
UI = 62.5ps
Opening: 24ps



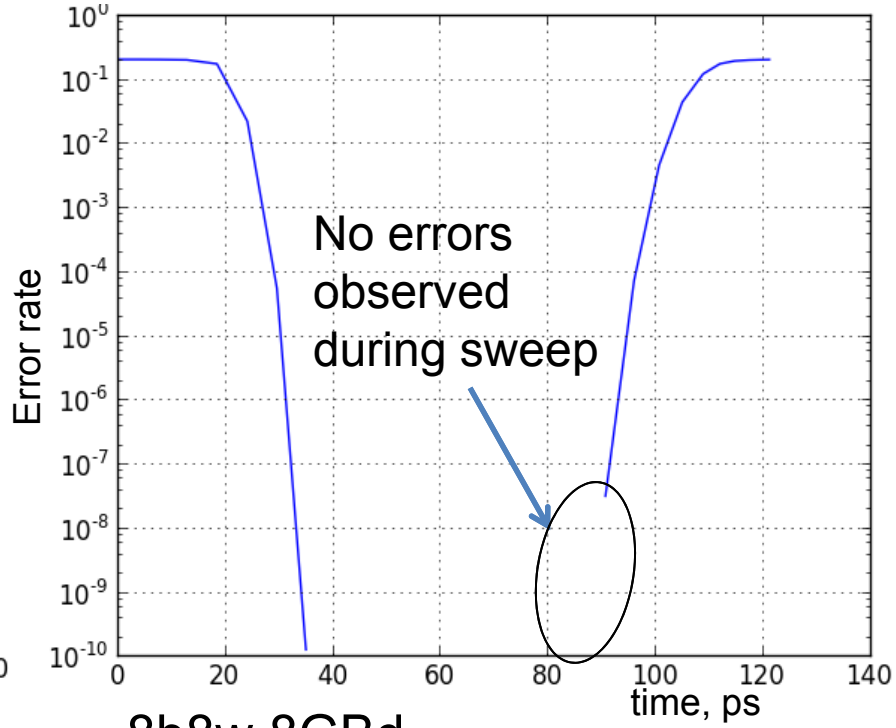
8b8w 8GBd
UI = 125ps
Opening: 50ps

Results

- Differential mode vs. 8b8w mode:
  - Measured bathtub plots at equivalent throughput (64Gb/s)



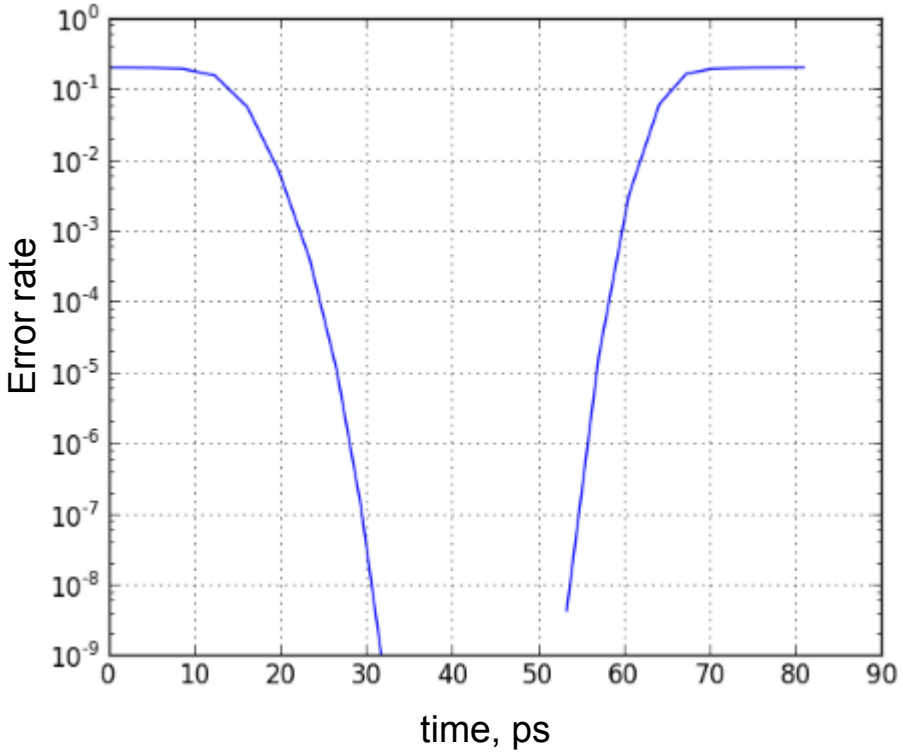
Differential 16GBd
UI = 62.5ps
Opening: 24ps

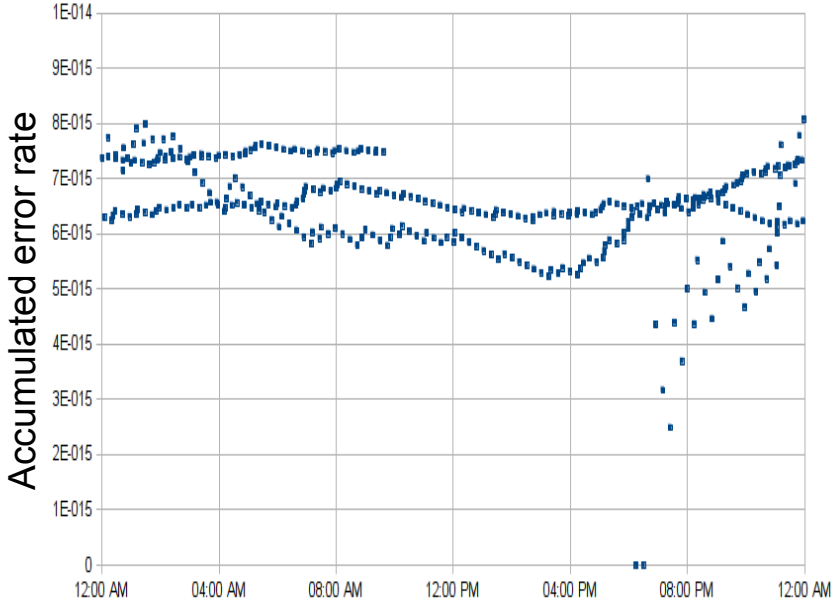


8b8w 8GBd
UI = 125ps
Opening: 50ps

Results

- Measured bathtub plot at 12GBd in 8b8w mode over medium loss channel (IL=15dB)



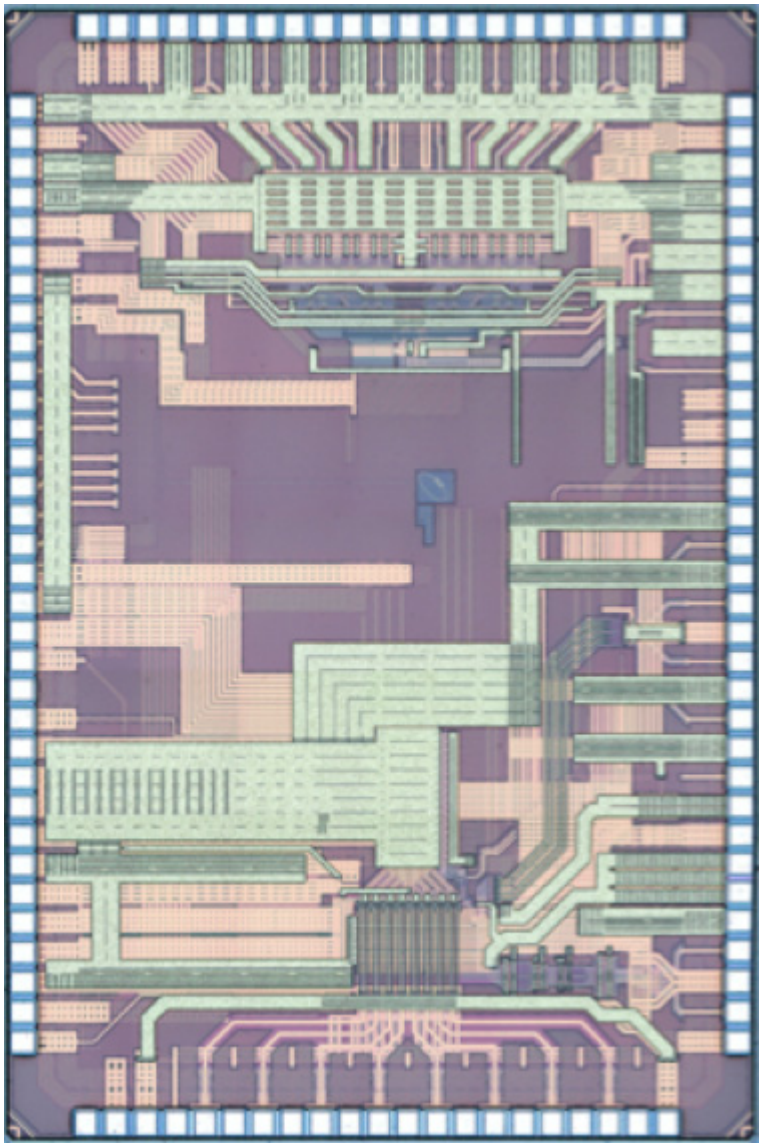


- Bit error counting tests run over weekend periods show an accumulated BER **better than $8e^{-15}$**

Results

- Extensive measurements have been made under various conditions:
  - Power supply noise
  - Common mode noise
  - Alien cross talk
  - Channel skew
- No significant degradation in BER is observed

Chip Micrograph and Features



Technology	40nm CMOS GP, VDD=0.9V, 10M, DGO
Package	Wire bond (1.5-2.0 mm length), COB
Channels	78cm, 55cm & 36cm Rogers (RO4450F/RO4350B), four 2.4mm connectors, 12” cables, loss up to 15dB
IO C_{die}	600fF, including ESD
Pads	Pitch 70µm, bond wire inductance = 1.5nH
Data Rate	8-12Gb/s/wire
Power and Energy Efficiency	412mW, 4.29 pJ/bit at 12Gb/s/wire
BER	< $8x10^{-15}$ at 12 Gb/s/wire
64b-encoder latency, area, power	0.5ns, 2000µm^2, 3mW
64b-decoder latency, area, power	0.5ns, 1330µm^2, 4mW
Differential legacy mode	Yes
Testability	Pattern generators (PRBS31, PRBS9), on-chip Eye Scope, error counters, SPI, analog test bus, test software
Per wire RX de-skew	1UI

Conclusion

- Successfully designed and tested a 8b8w-Coded SerDes link in 40nm
- Demonstrated BER performance < 10^{-14} up to 12Gb/s/wire
- Demonstrated receiver circuits that can de-skew up to 1UI and are robust under common-mode and power supply noise conditions
- Demonstrated approximately 2x advantage in power and eye-opening over legacy differential links at equivalent throughput over same number of wires

References

- [1] D. Slepian, “Permutation Modulation Codes”, Proceedings of the IEEE, vol. 53, No. 3, 228-236, 1965.
- [2] J. Lee, M. Chen, and H. Wang, “Design and Comparison of Three 20-Gb/s Backplane Transceivers for Duobinary, PAM4, and NRZ Data”, *JSSC, Vol. 43, No.9, Sep.2008.*
- [3] A. Amirkhany, et al, “4.1pJ/b 16Gb/s Coded Differential Bidirectional Parallel Electrical Link”, *ISSCC Dig. Tech. Papers, pp. 138-139, Feb. 2012.*
- [4] H. Cronie, A. Shokrollahi, and A. Tajalli, "Methods and Systems for Noise Resilient and Low Power Communications with Sparse Signaling Codes," *US Patent Application Number US2012/0213299 A1.*
- [5] S. Zogopoulos and W. Namgoong “High-Speed Single-Ended Parallel Link Based on Three-Level Differential Encoding ”, *JSSC, Vol. 44, No.2, Feb.2009.*

Thank you

A 25.6Gb/s Differential and DDR4/GDDR5 Dual-Mode Transmitter with Digital Clock Calibration in 22nm CMOS

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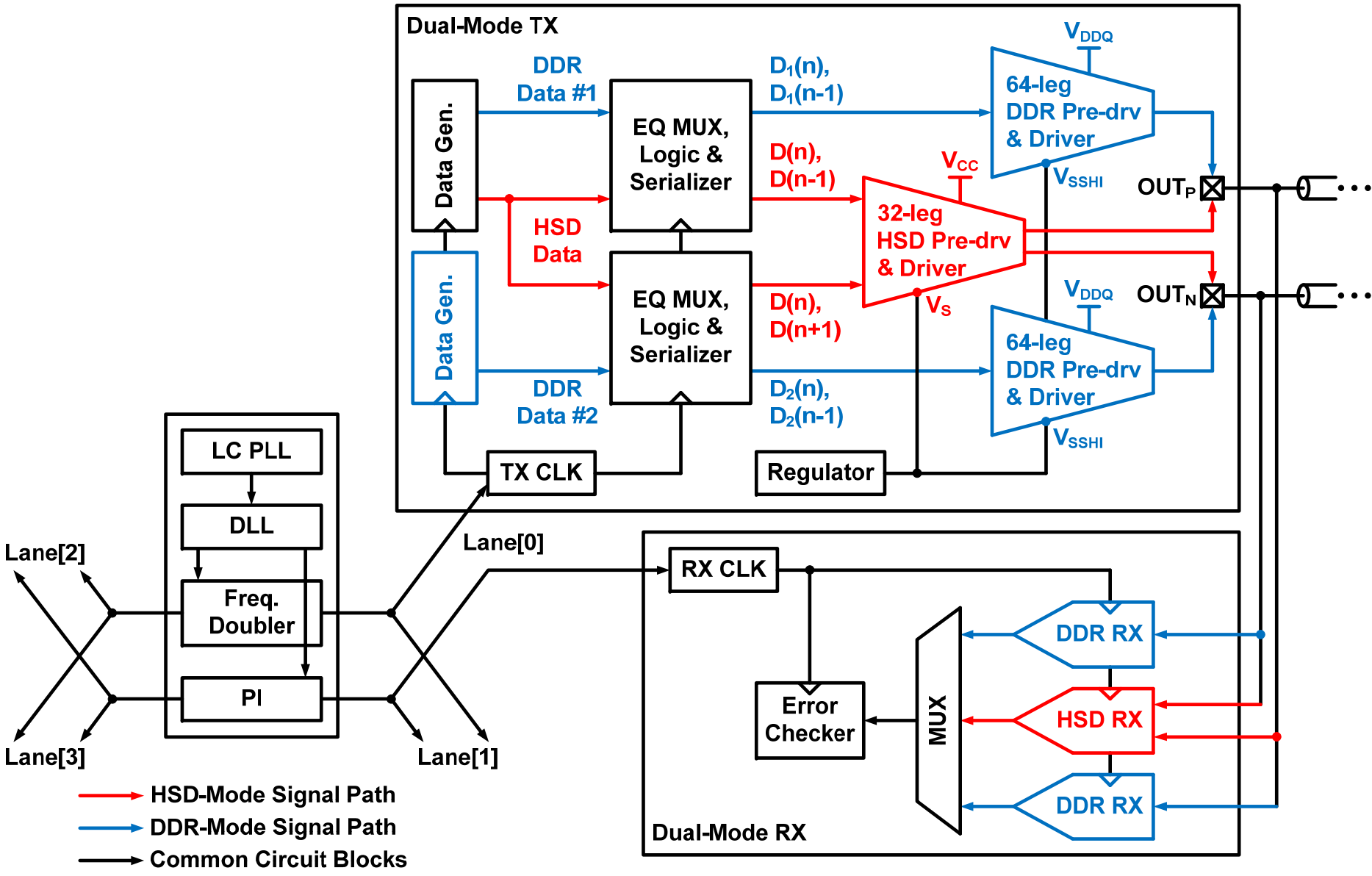
Outline

- Motivation
- Dual-mode XCVR architecture
  - High-speed differential mode (HSD)
  - DDR4/GDDR5 mode (DDR)
- Features and implementation
- Measurement results
- Summary

Motivation

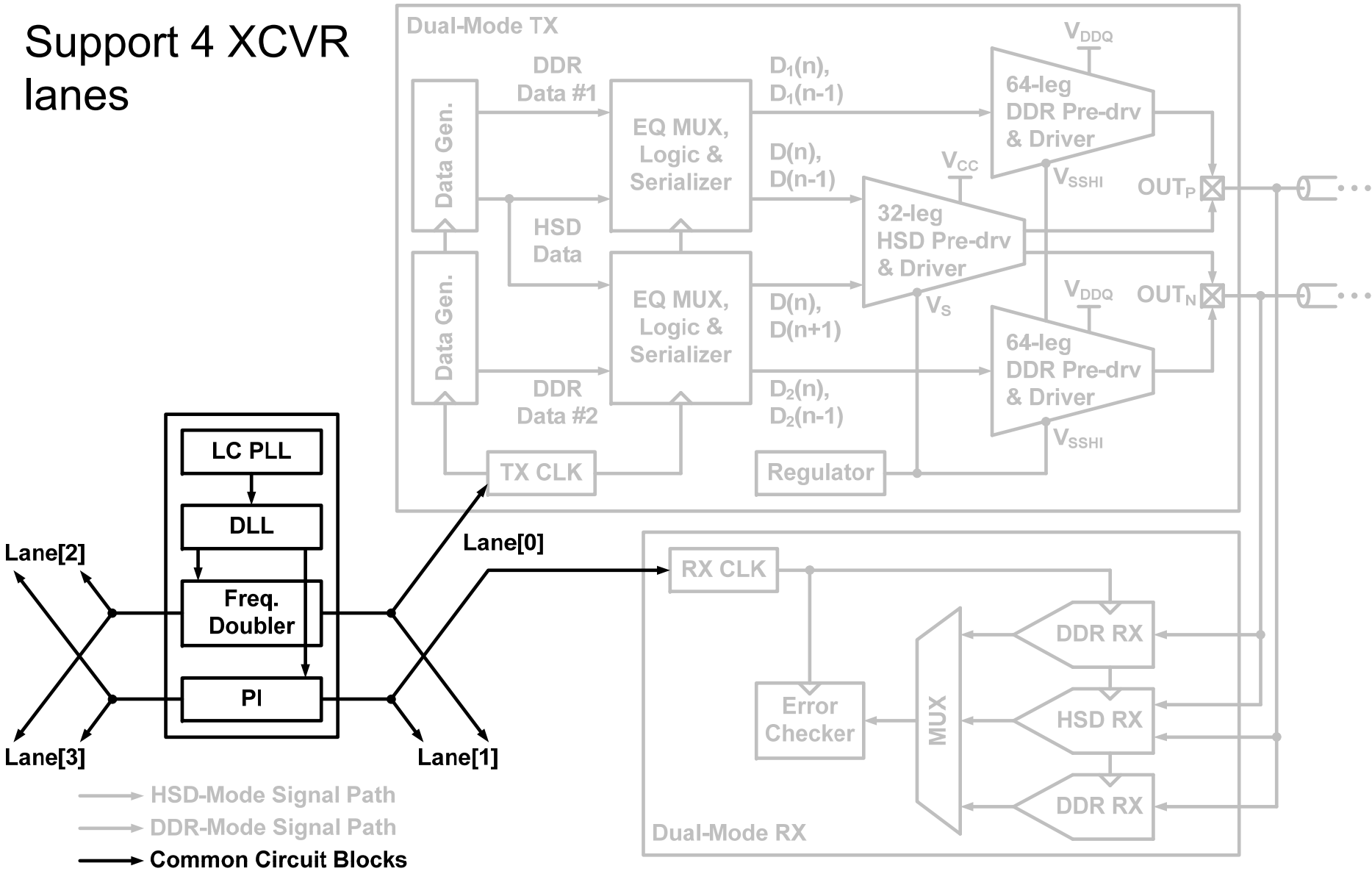
- Unified memory I/O designs for
  - Multiple memory specs
  - Legacy compatibility
  - Performance scalability
  - Low power & small area
- Challenges
  - Varieties of signaling specs
  - High-voltage tolerance techniques
  - Area and channel loss overheads

Dual-mode Bi-directional XCVR

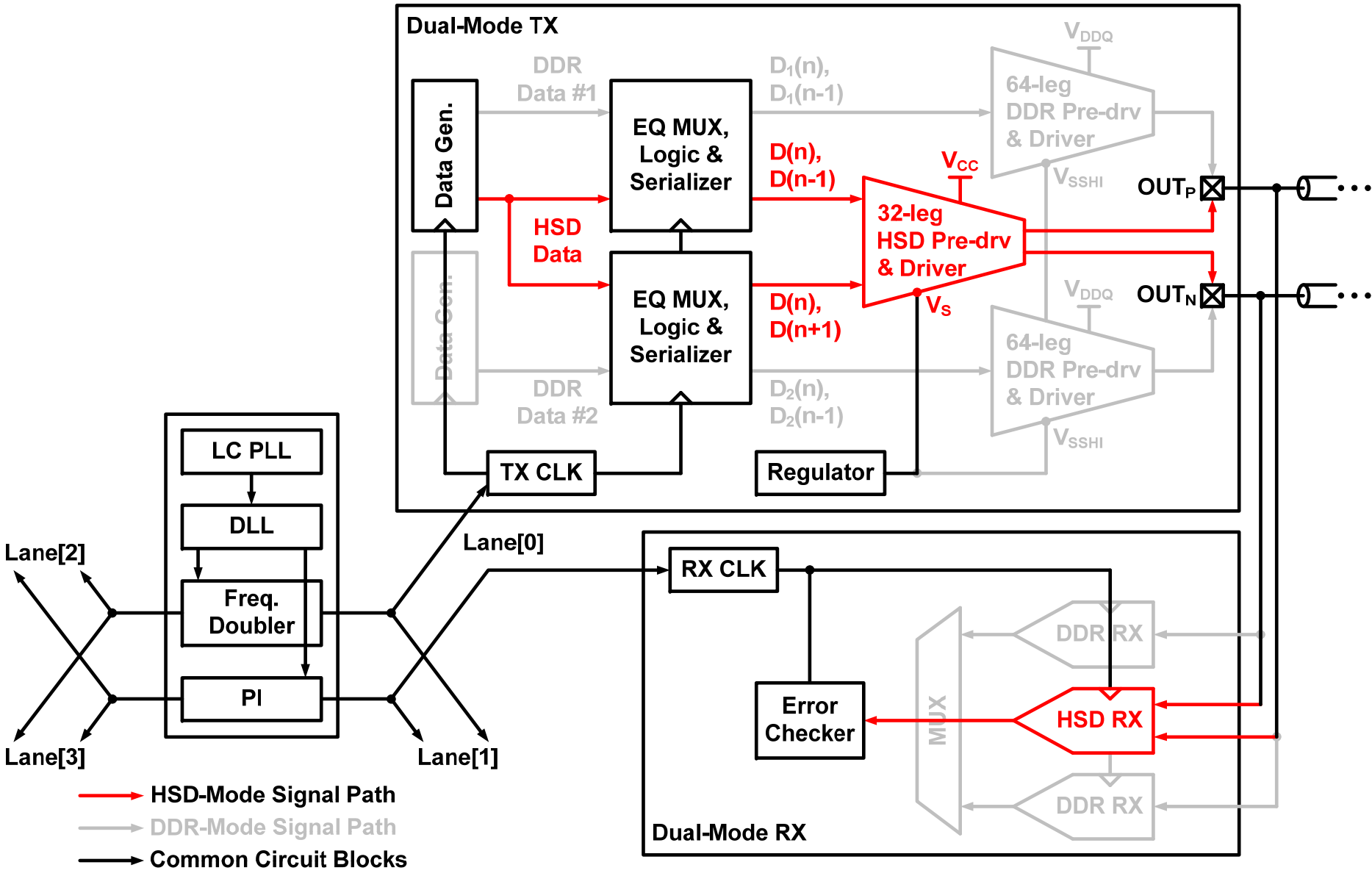


Global Clocking

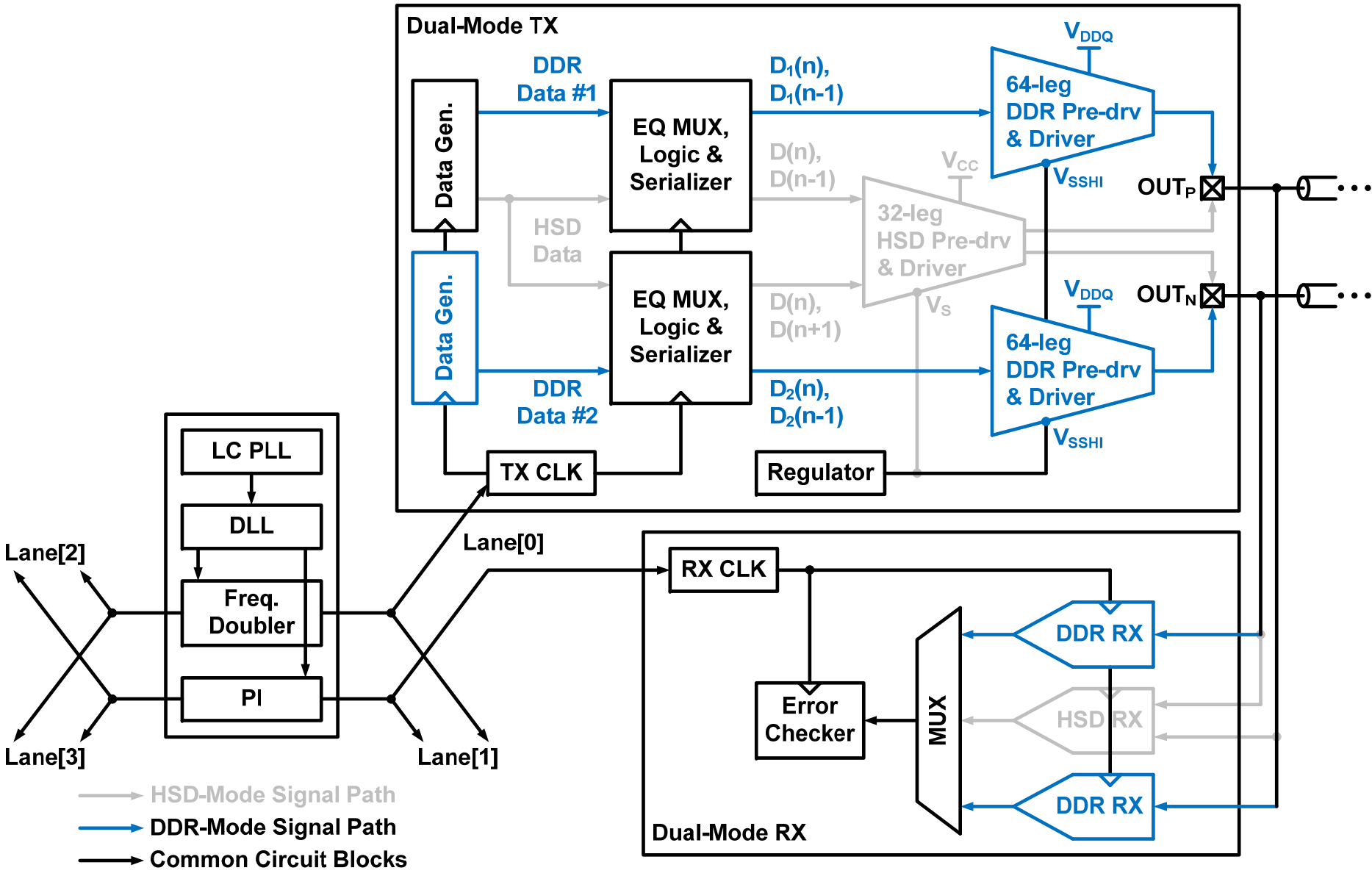
- Support 4 XCVR lanes



HSD-mode Bi-directional XCVR

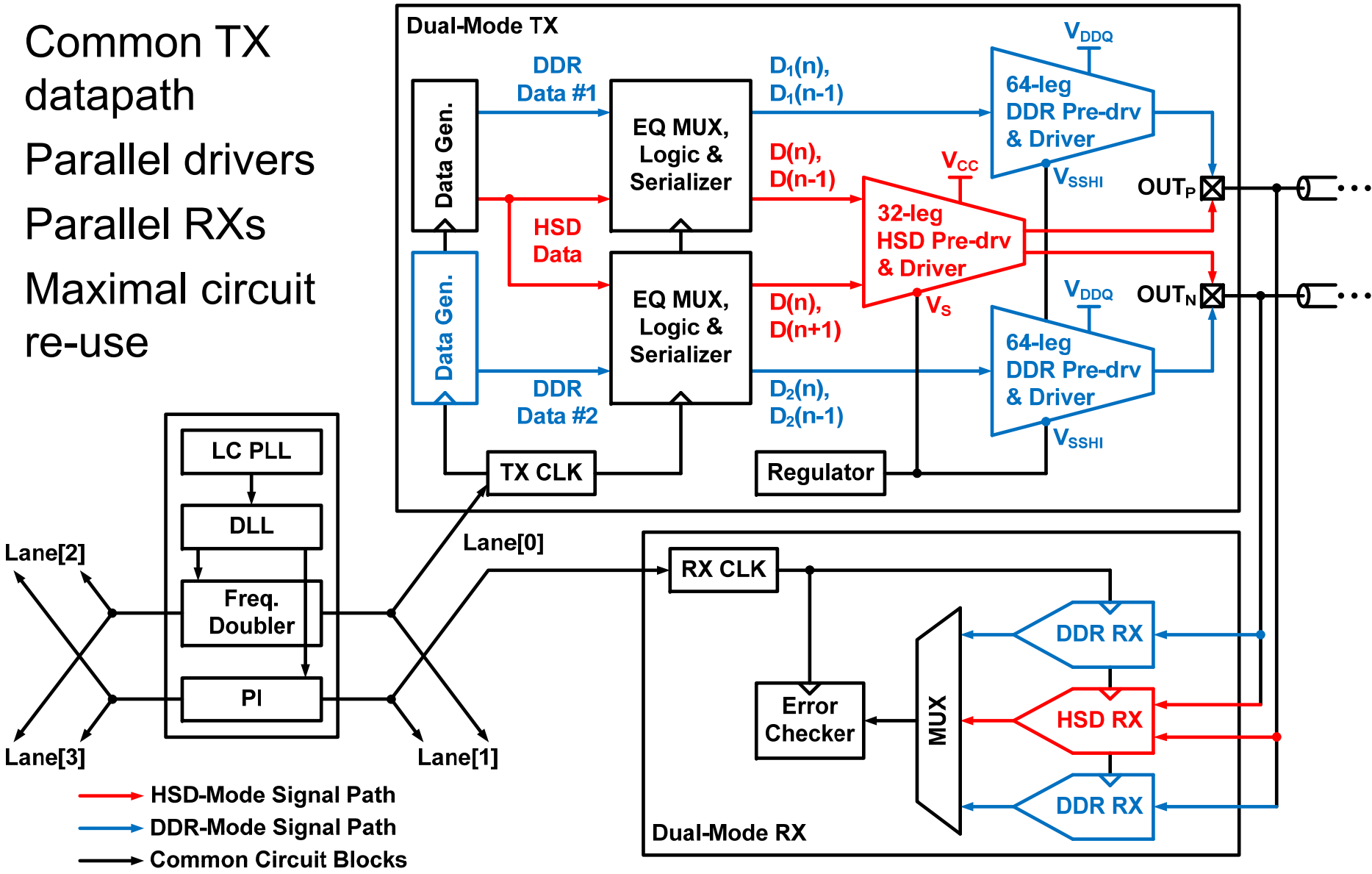


DDR-mode Bi-directional XCVR



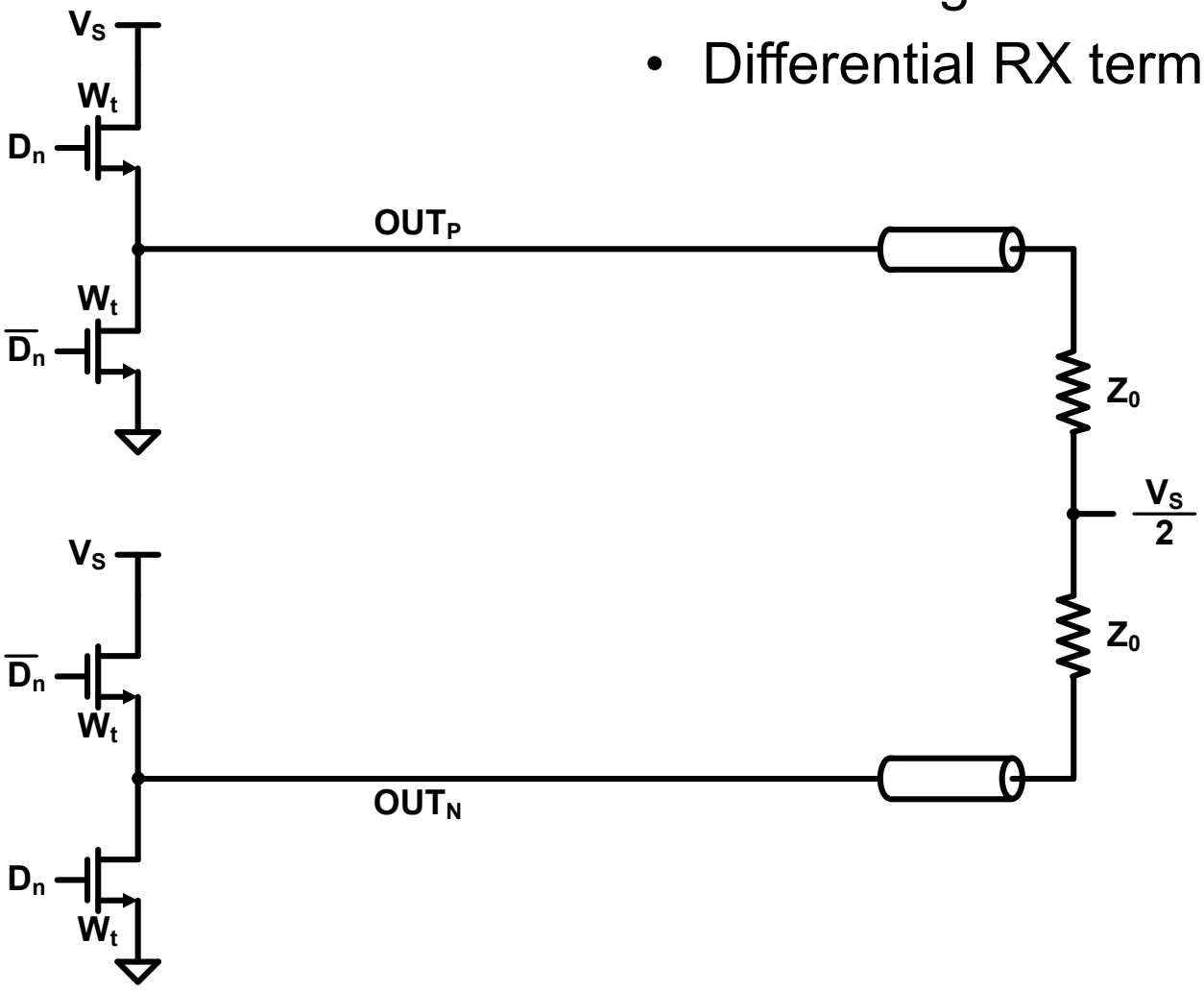
Dual-mode Bi-directional XCVR

- Common TX datapath
- Parallel drivers
- Parallel RXs
- Maximal circuit re-use



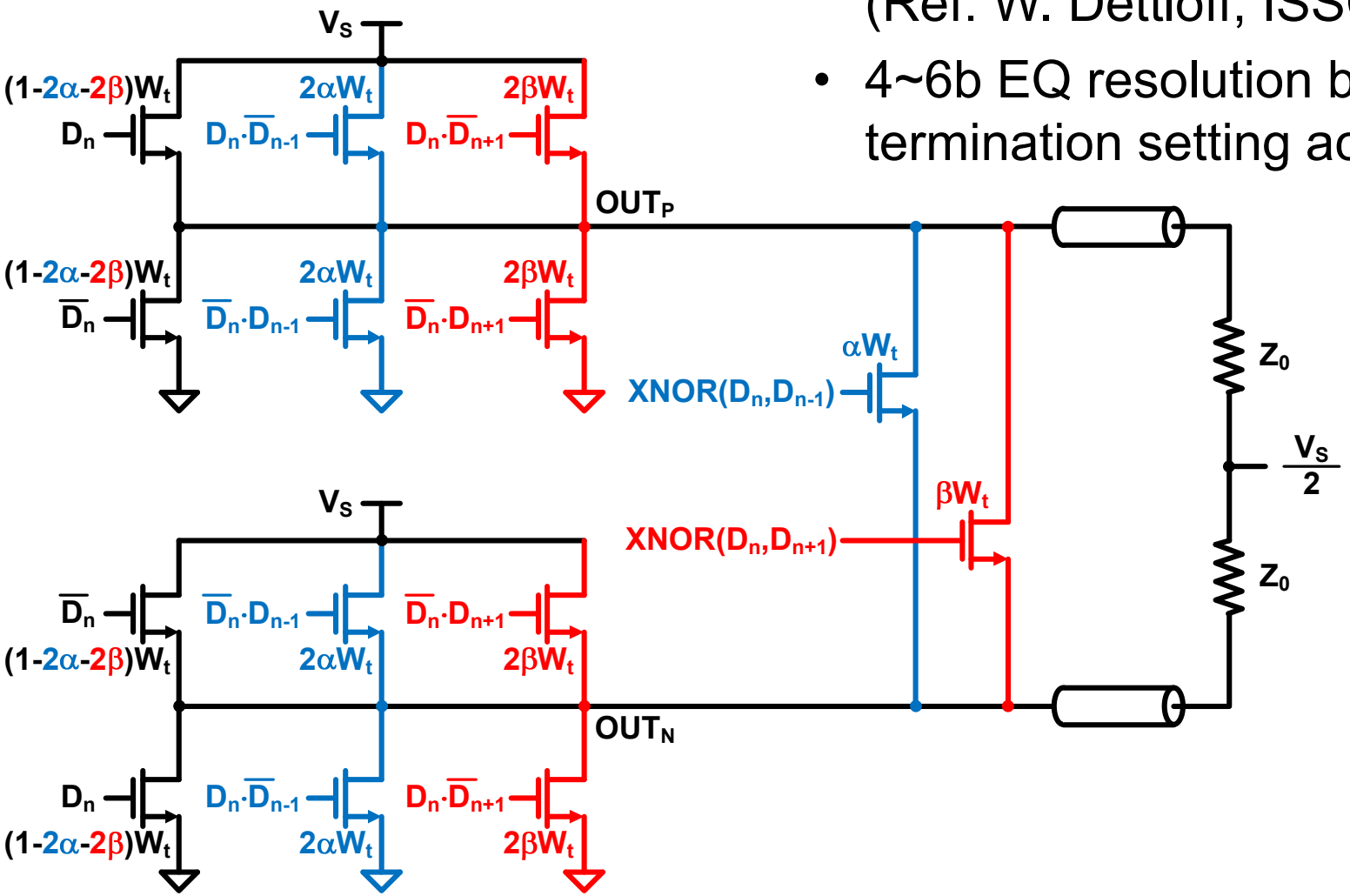
HSD-mode SST Driver

- Fully NMOS differential driver
- Low swing
- Differential RX termination



HSD-mode 3-tap EQ SST Driver

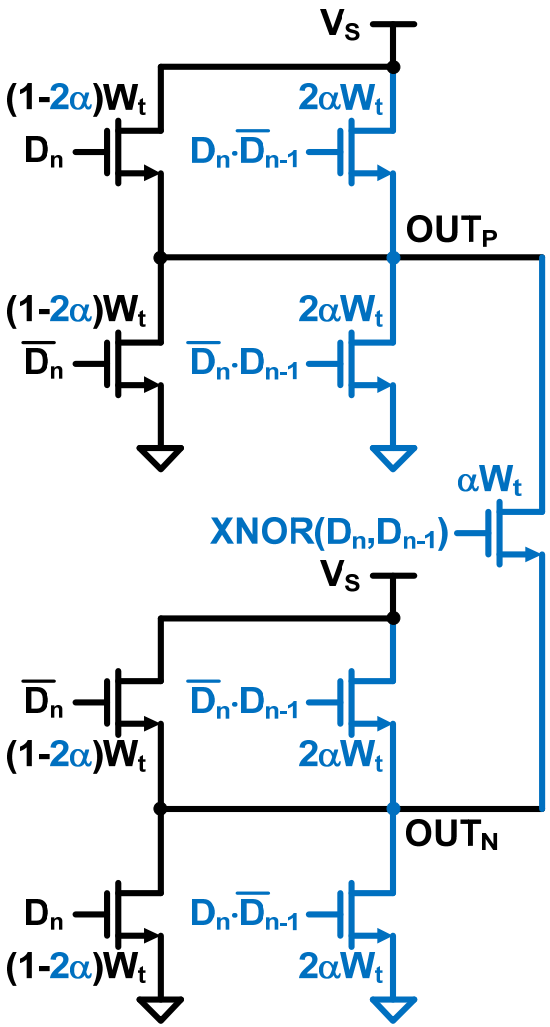
- Shorting path eliminates duplicate current consumption (Ref: W. Dettloff, ISSCC 2010)
- 4~6b EQ resolution based on TX termination setting across PVT

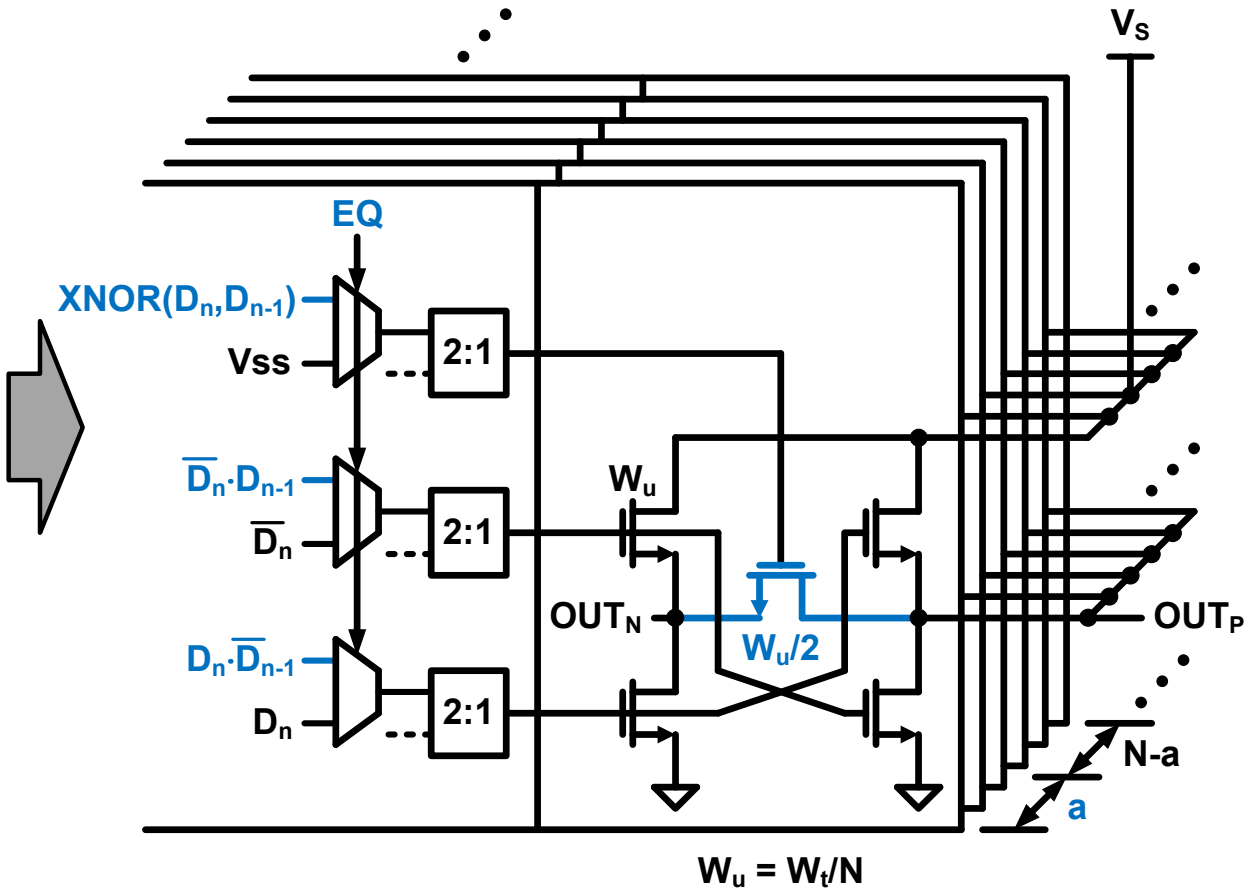


HSD-mode EQ & Term. Controls

Ex: 2-tap EQ to simplify illustration

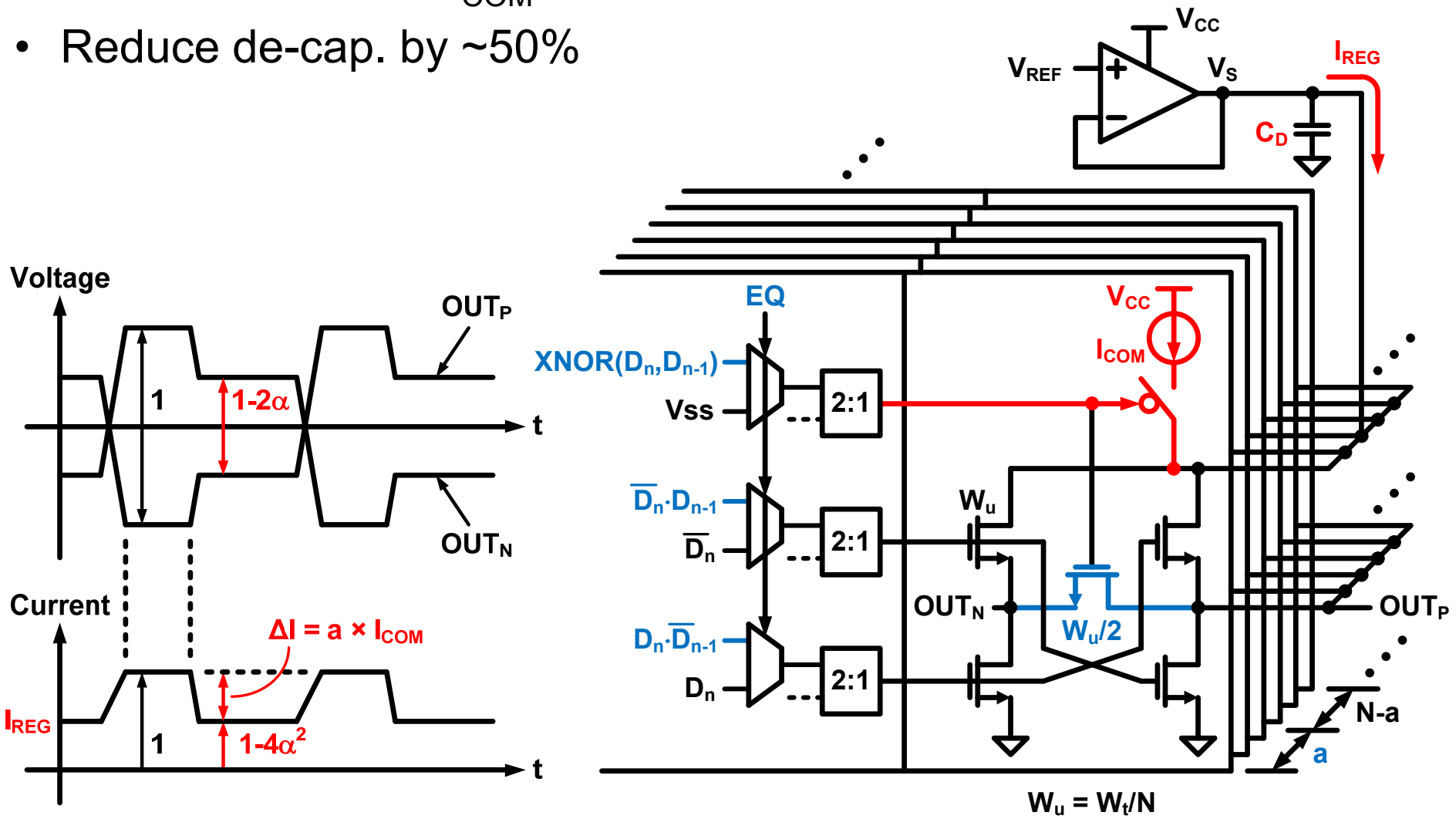
- Enable ‘N’ legs for TX term. (max. 32 legs)
- ‘a’ legs for post-cursor, $\alpha = a/(2N)$
- ‘N-a’ legs for cursor





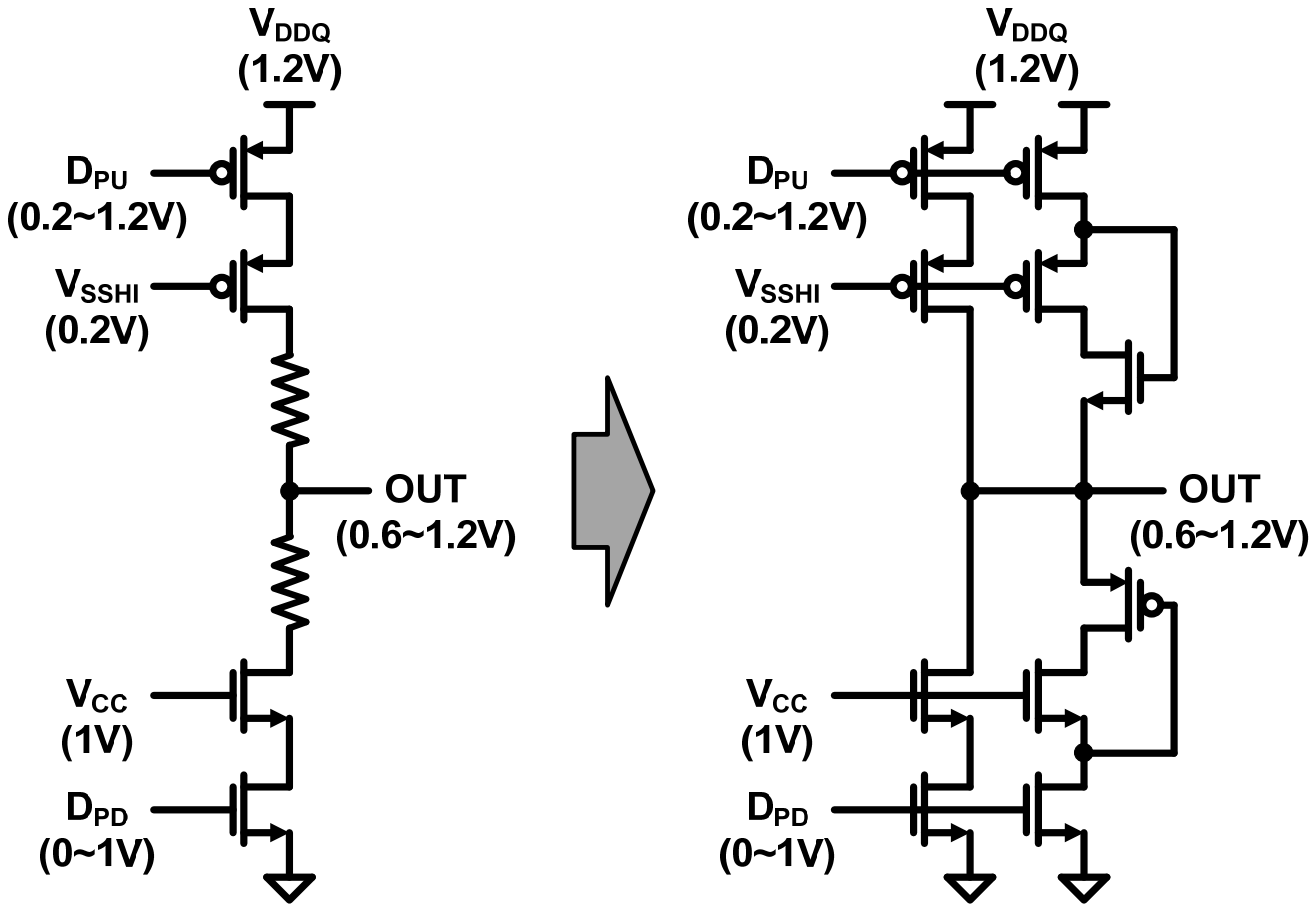
HSD-mode Driver Supply Regulation

- Minimize self-induced noise by injecting data-dependent current
- 5-bit DAC controls I_{COM} bias
- Reduce de-cap. by ~50%



DDR-mode SST Driver

- Conventional passive linear resistance driver (left)
- All thin-gate-oxide linear resistance driver (right)
- Both have cascode devices for HV tolerance



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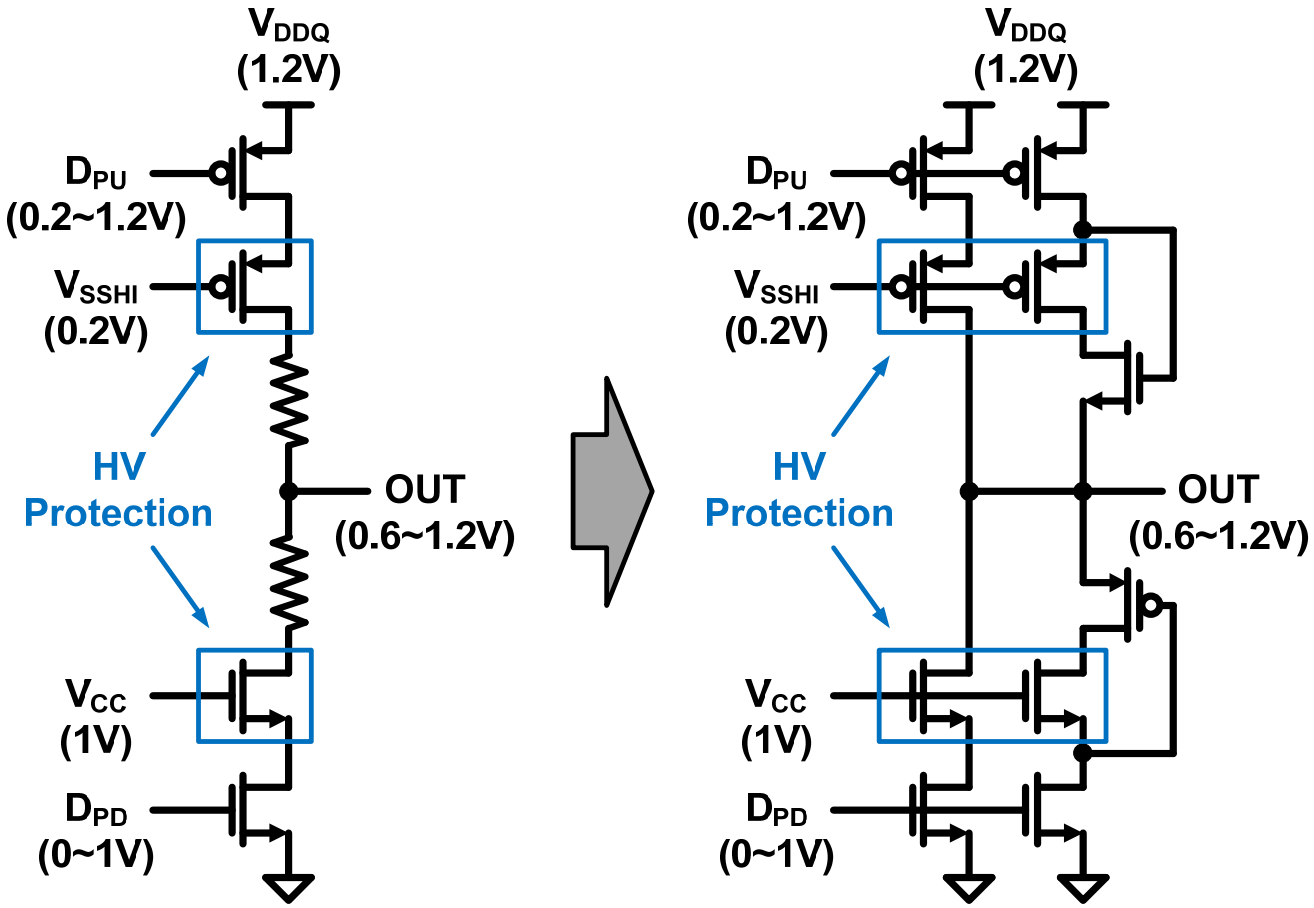
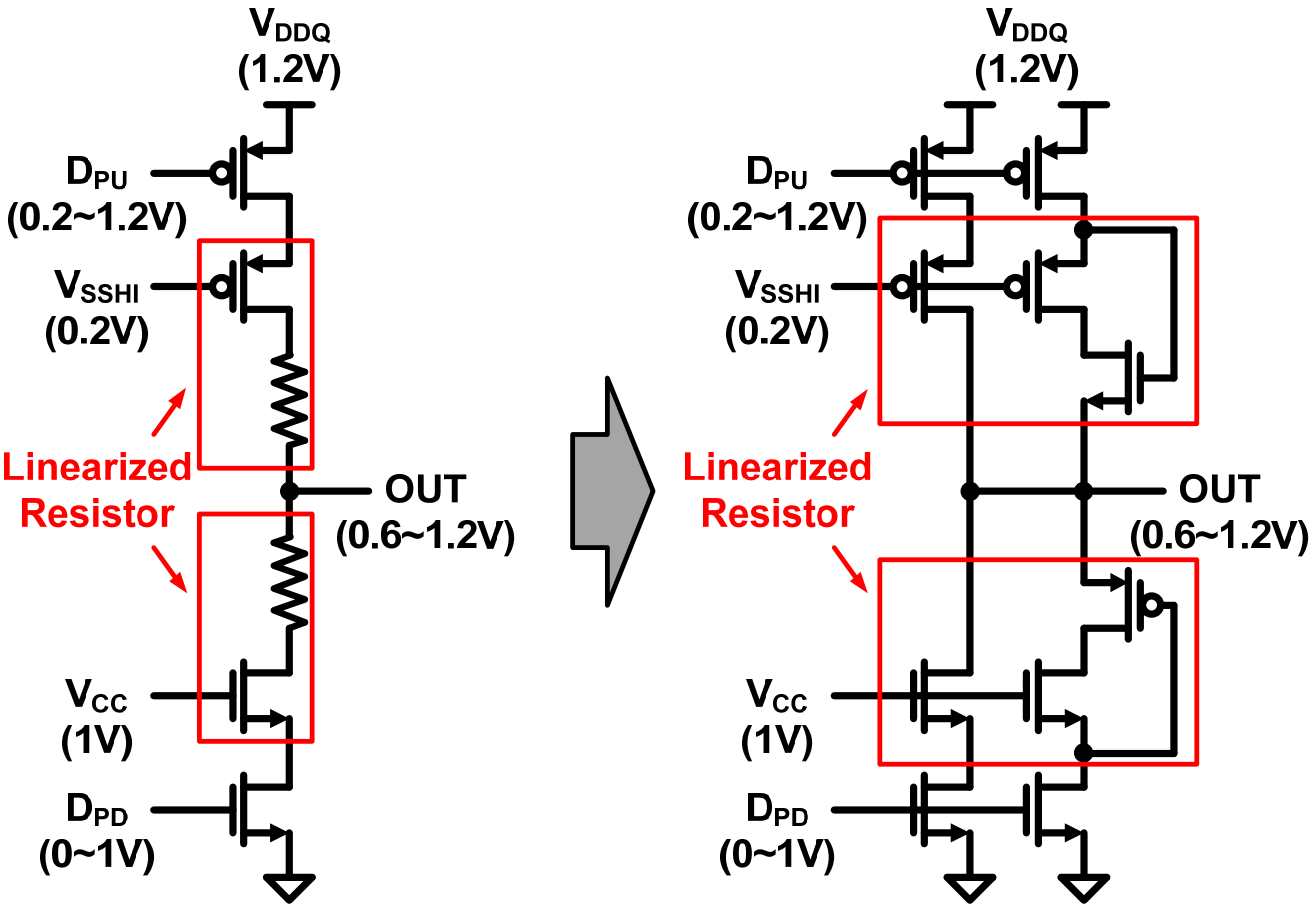


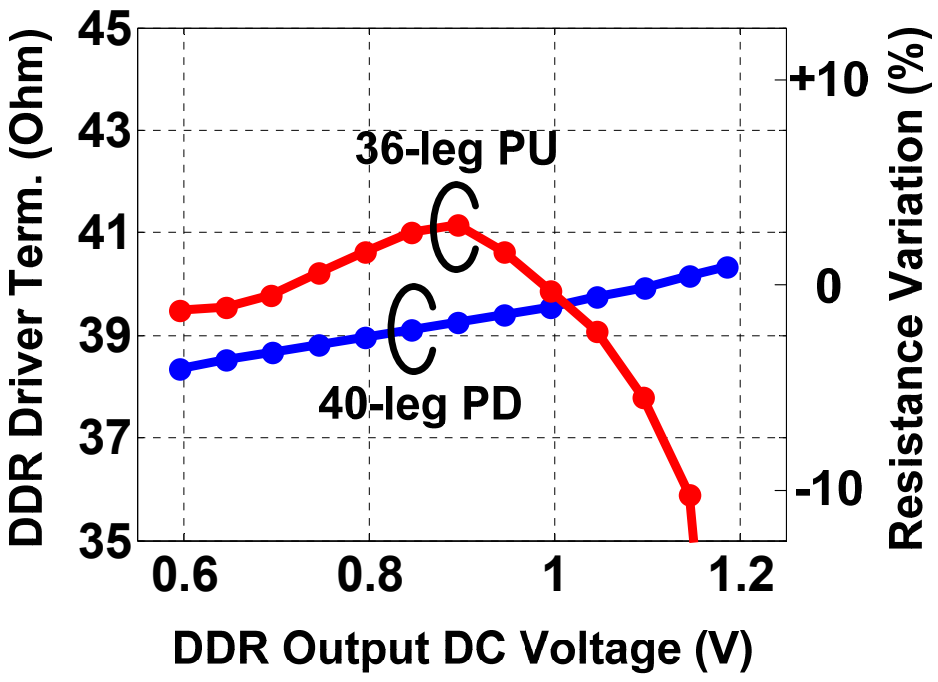
DDR-mode SST Driver

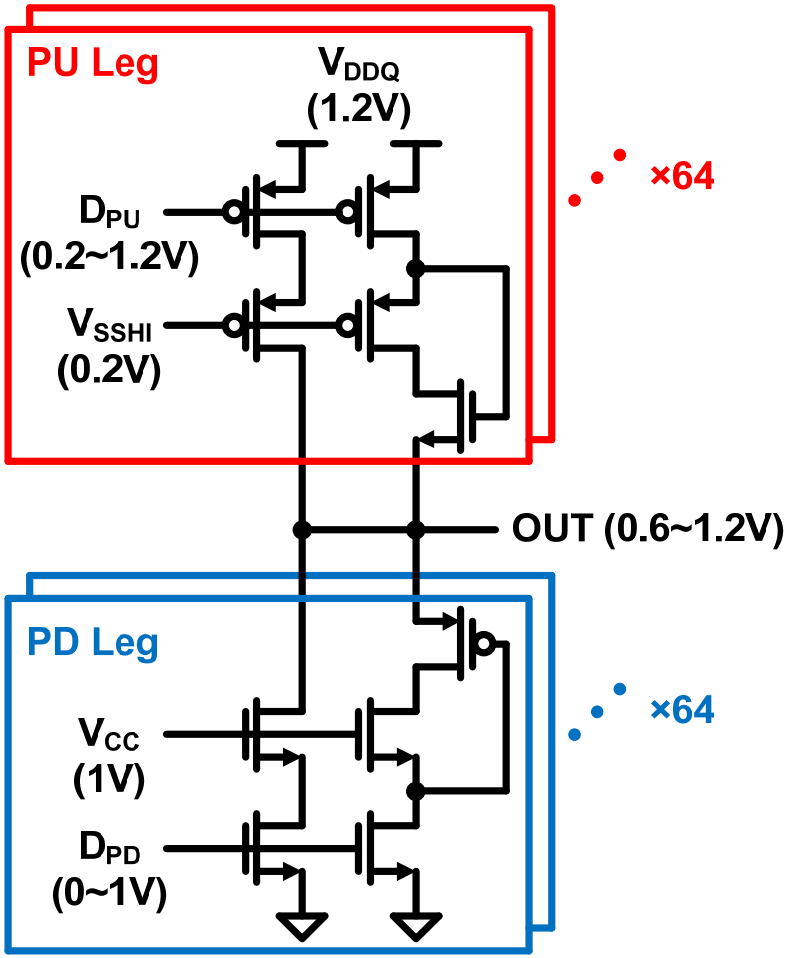
- Complementary P/N triode-/diode-connection devices enable resistance linearization without extra bias for HVT
- Reduce area and metal routing by >50%
- Pad capacitance reduction & less resistance process variation



DDR Driver Resistance Measurement

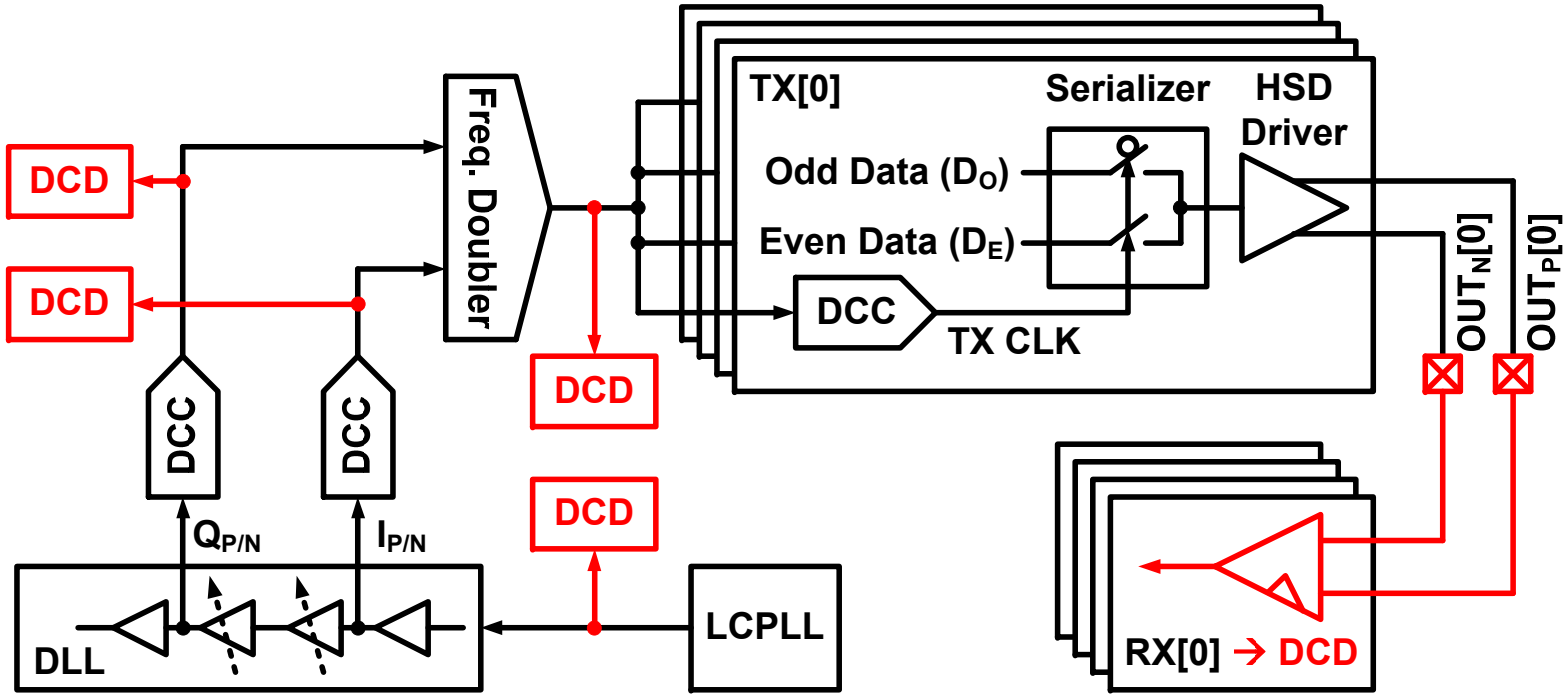
- < ±10% resistance variation over 0.5~0.95V_{DDQ} swing



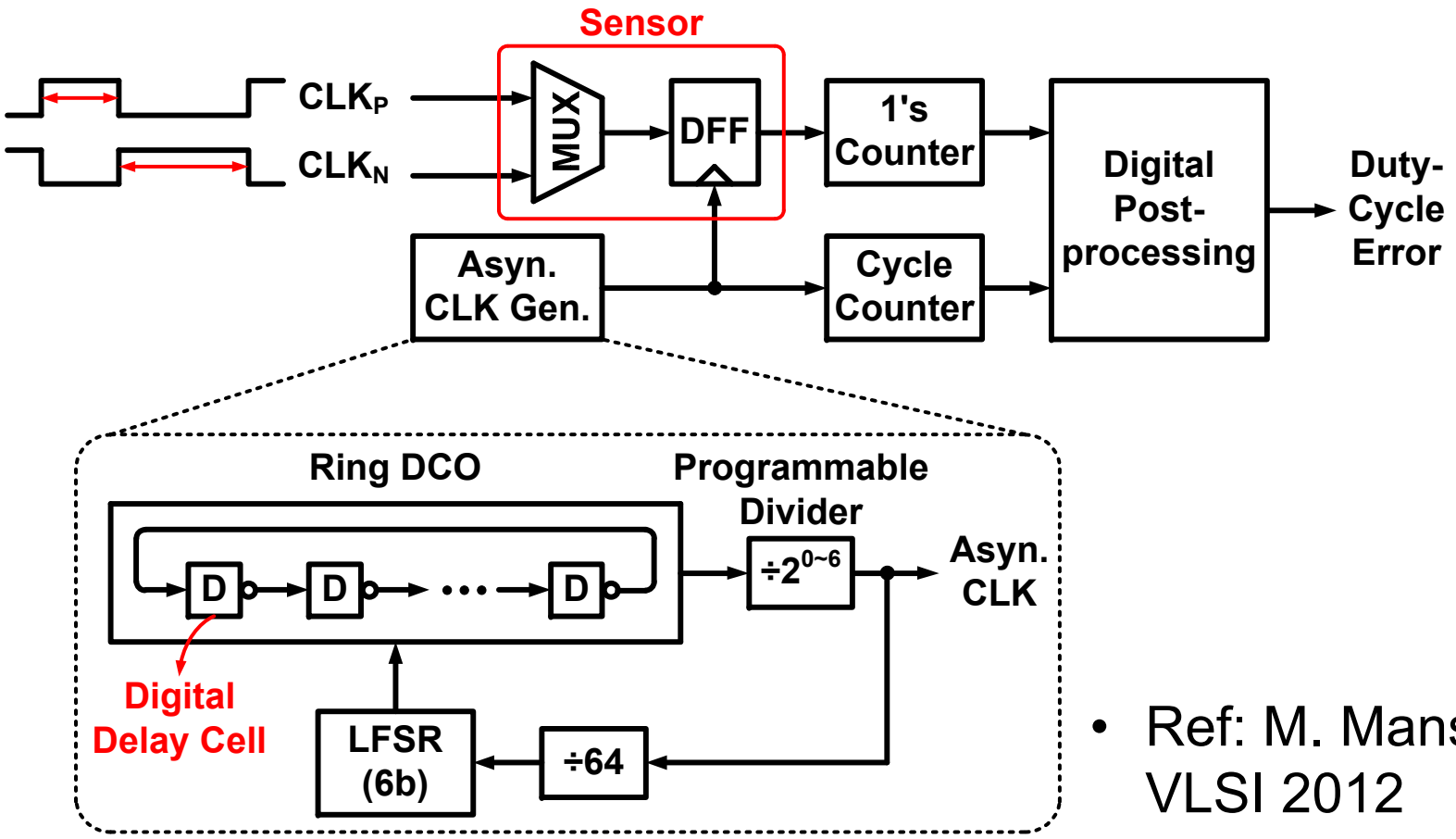


TX Clock Duty-Cycle Calibration

- Sequential, multi-stage clock calibration
- Calibration comprehends all circuits in TX datapath
  - ➢ Use RX in bi-directional transceiver as duty-cycle detector
- I-DAC based DCC
  - ➢ Range control supports ±3%~±8%, 7-bit resolution



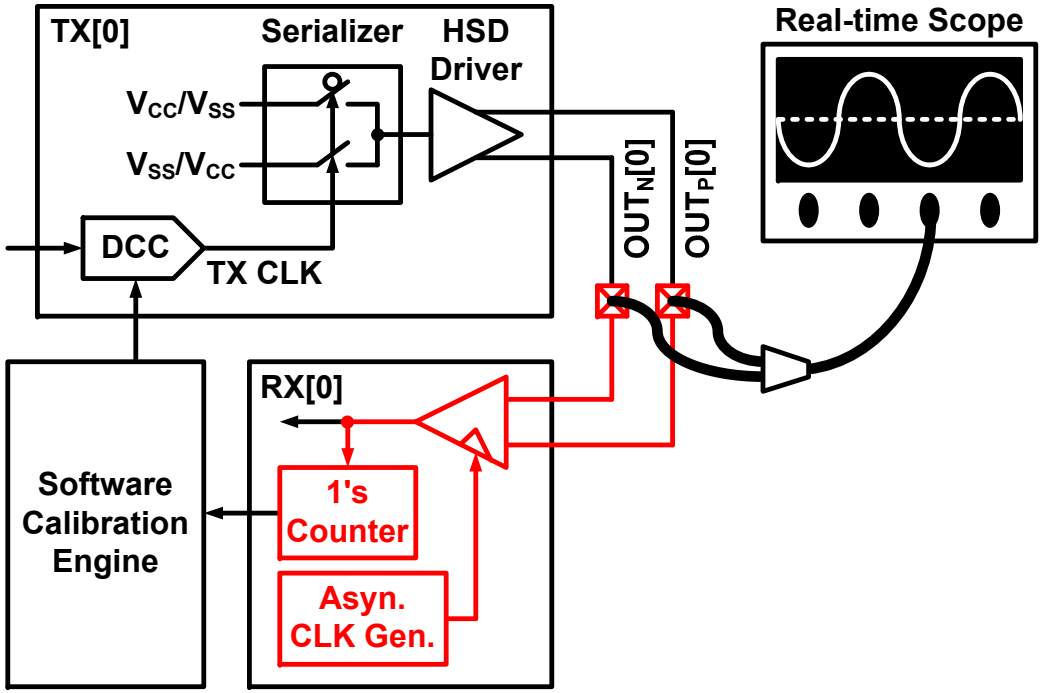
Digital Duty Cycle Detector (DCD)



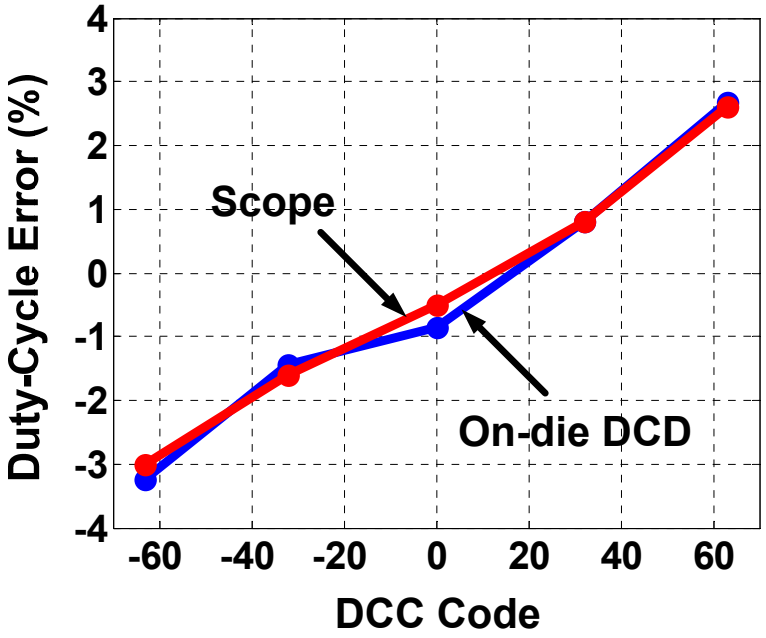
- Ref: M. Mansuri, VLSI 2012

- Based on Random Equivalent-Time Sampling (RETS)
- DCE = Difference in ones counts of CLK_P & CLK_N samples
- Differential measurement cancels sensor non-idealities

TX DCC & DCD Measurements



- High resolution setting



- TX output duty-cycle calibrated through loopback RX
- On-die measurements correlate with scope measurements
  - Error < 0.36%

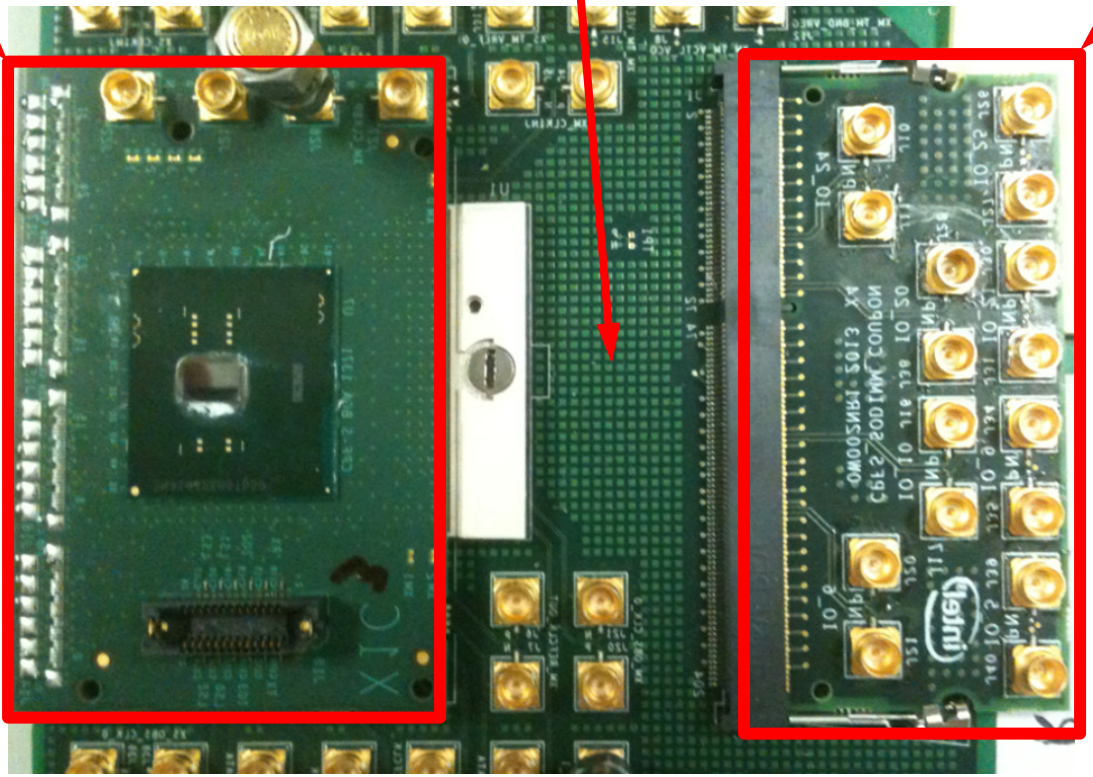
Test Setup

- Demonstrate potential circuit and package unification for
  - DDR4/GDDR5 (DDR mode)
  - High-speed differential serial I/O (HSD mode)

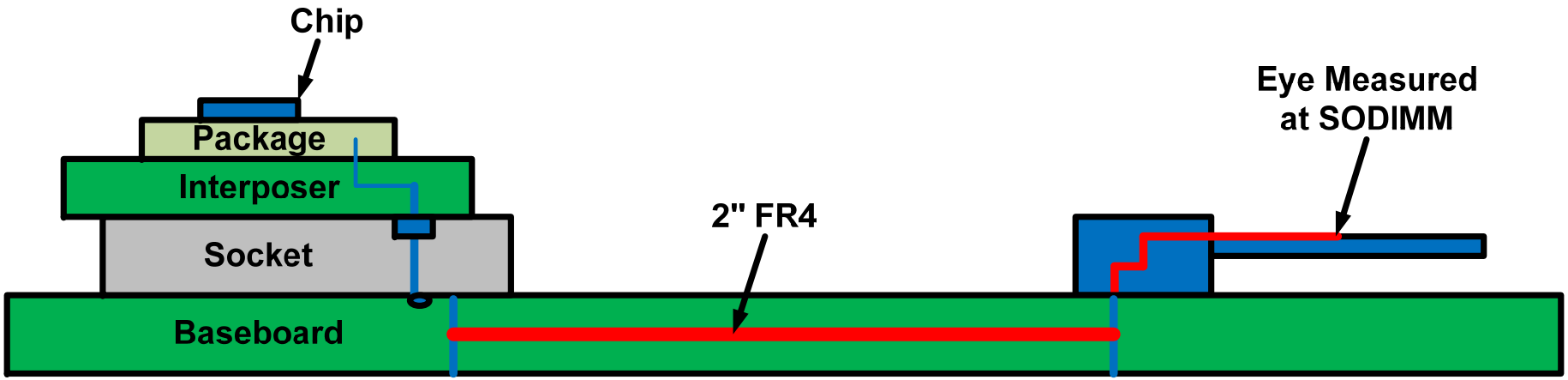
Package on HDI Interposer + PGA Socket

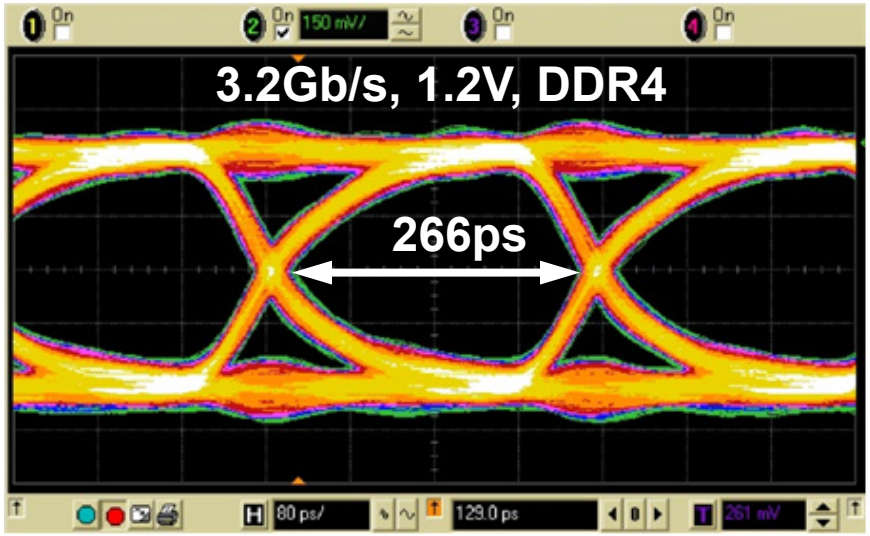
Internal FR4 traces

SODIMM Connector + Plugin Card



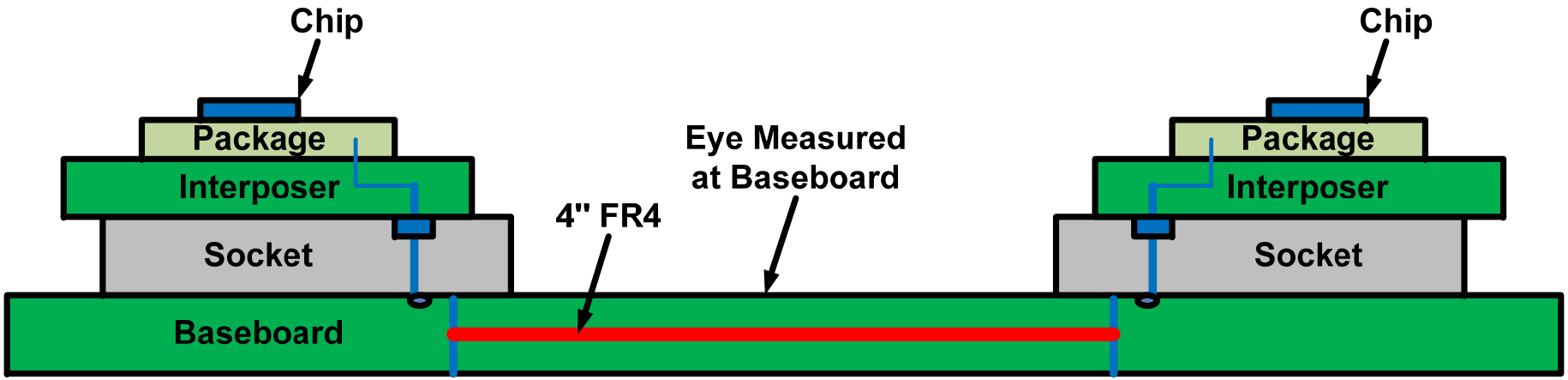
DDR-mode Measurement Result

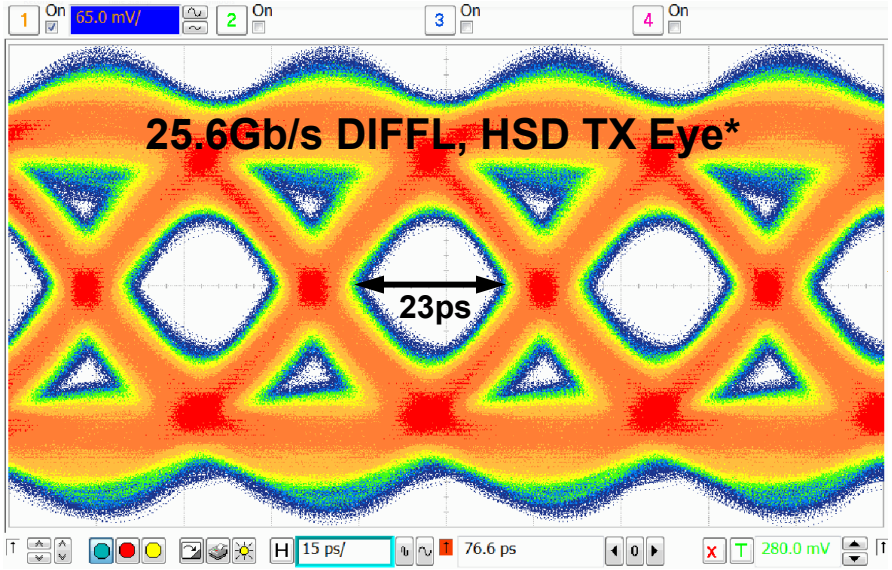


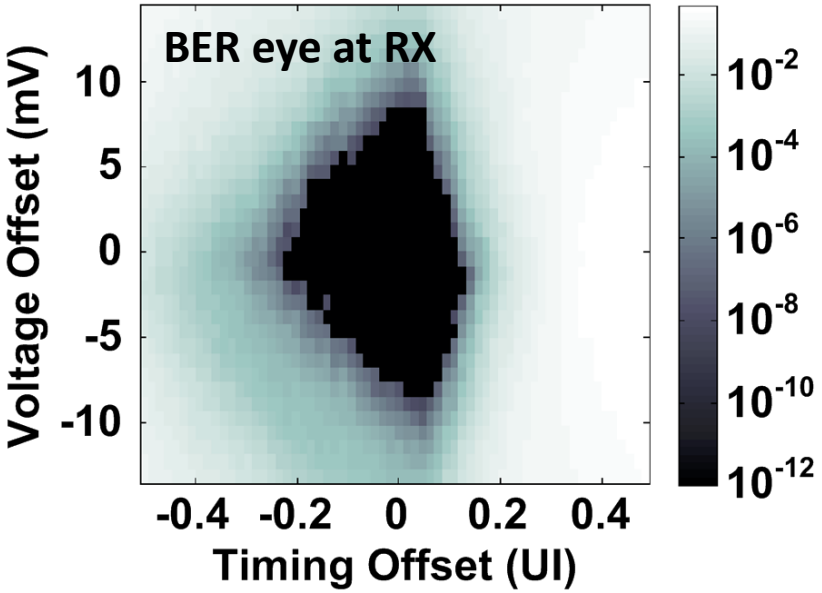


- Robust Eye Margins for both DDR4 & GDDR5

HSD-mode Measurement Result



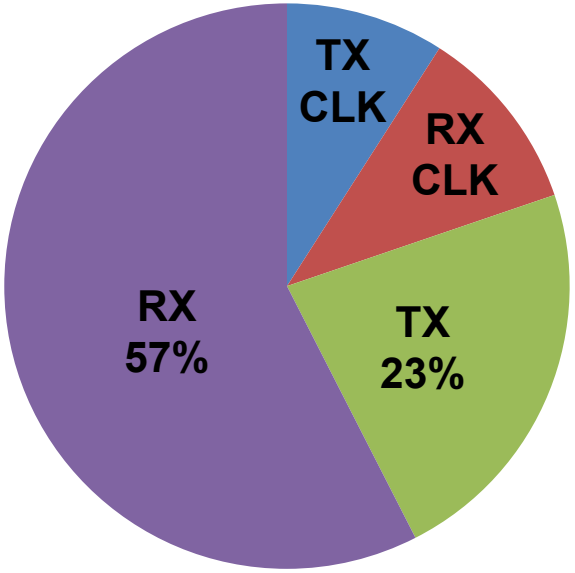




- Demonstrated 25.6Gb/s serial I/O over 24dB loss channel w/ unified XCVR + Package

Measurement Result Summary

- Power breakdown @25.6Gb/s per XCVR lane:



- TX & RX clock powers are amortized over 4 XCVR lanes
- HSD RX includes CTLE & DFE (Ref: J. Jaussi, ISSCC 2014)

Technology	22nm		
Mode	DDR4	GDDR5	HSD
Supply	V_{CC}=0.8V V_{DDQ}=1.2V	V_{CC}=0.9V V_{DDQ}=1.5V	V_{CC}=1.05V
Aggregate BW per Lane	6.4Gb/s (3.2×2)	12.8Gb/s (6.4×2)	25.6Gb/s (25.6×1)
Channel Loss @ Nyquist Freq.	2dB @1.6GHz	5dB @3.2GHz	24dB @12.8GHz
TX Output Swing	660 $mV_{pp\text{-}se}$	830 $mV_{pp\text{-}se}$	500 $mV_{pp\text{-}diff}$
TX RMS Jitter*	2.4ps	1.9ps	820fs
TX Energy Efficiency	2.5pJ/b	2.2pJ/b	1.1pJ/b
Link Energy Efficiency**			4.8pJ/b
TX Area w/ Regulator Cap.	135µm × 40µm		
Pad Capacitance	450fF		

* Measured after package, interposer, socket & 2” FR4
** Excludes the LC-VCO PLL

Summary

- A unified DDR4/GDDR5 & HSD transceiver enables aggressive post-DDR4 memory I/O scaling with backward compatibility
  - 3.2Gb/s, 1.2V, DDR4
  - 6.4Gb/s, 1.5V, GDDR5
  - 25.6Gb/s, HSD, 4.8pJ/b, 24dB channel loss
- Several circuit techniques minimize power and area overheads

Acknowledgements

The authors would like to thank

- B. Horine and M. Leddige for package and interconnect design;
- V. Baca and M. Balasubramanian for layout;
- P. Parmar, Y. Fan, A. Martin, S. Thakare, K. Aygun, A. Zhang, P. Stolt, D. Dunning, J. McCall, D. Conrow, and V. Ragavassamy for design support;
- R. Mooney, M. Haycock and W.-H. Wang for project management.

An 8-to-16Gb/s 0.65-to-1.05pJ/b 2-Tap Impedance-Modulated Voltage-Mode Transmitter with Fast Power-State Transitioning in 65nm CMOS

Young-Hoon Song[1], Hae-Woong Yang[1], Hao Li[2],
Patrick Chiang[2,3], and Samuel Palermo[1]

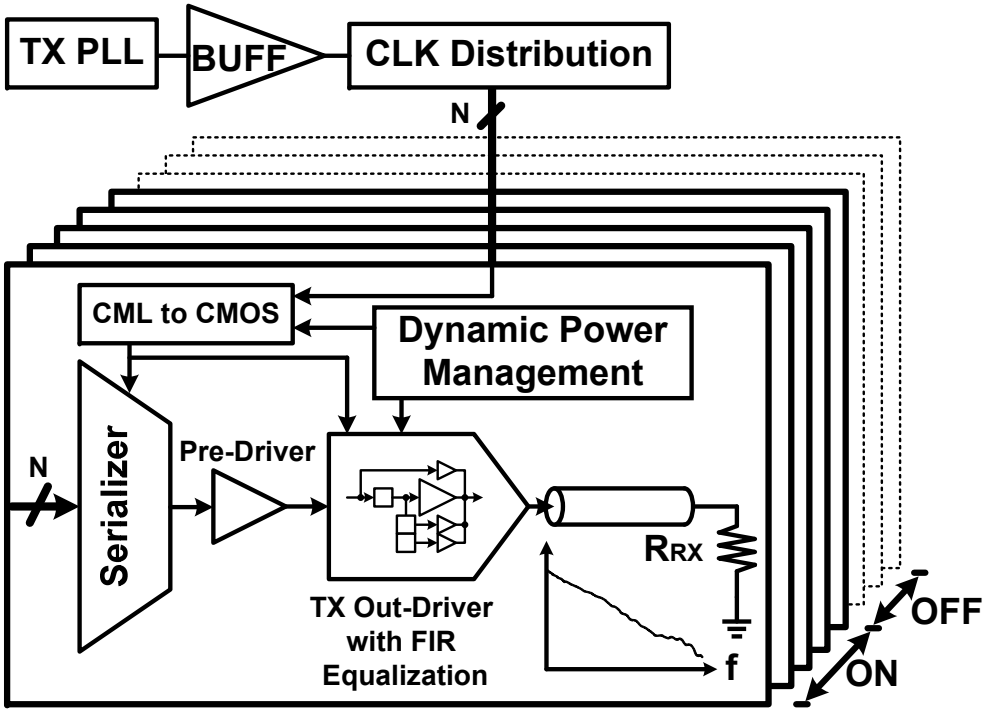
[1] Texas A&M University, College Station, TX
[2] Oregon State University, Corvallis, OR
[3]Fudan University, Shanghai, China

Outline

- Low-power transmitter design challenges
- Low-power transmitter design details
- Measurement results
- Conclusion

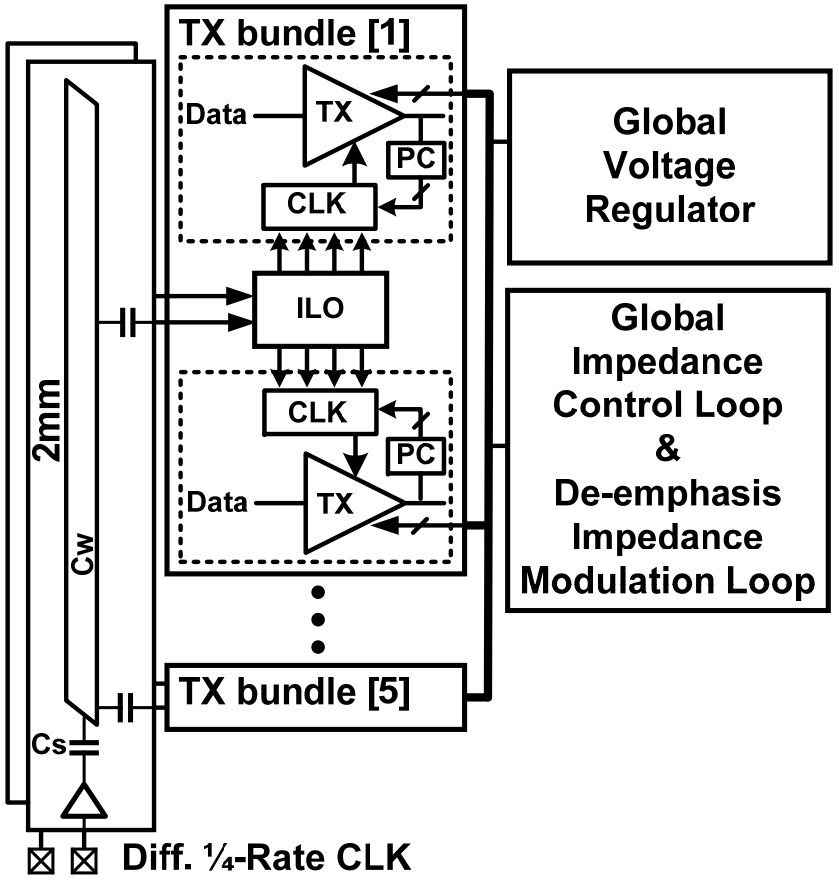
Low-Power TX Challenges

- Clocking Power
- Digital Serializer and Pre-driver Power
- Channel Loss
- Dynamic Power Management (DPM)

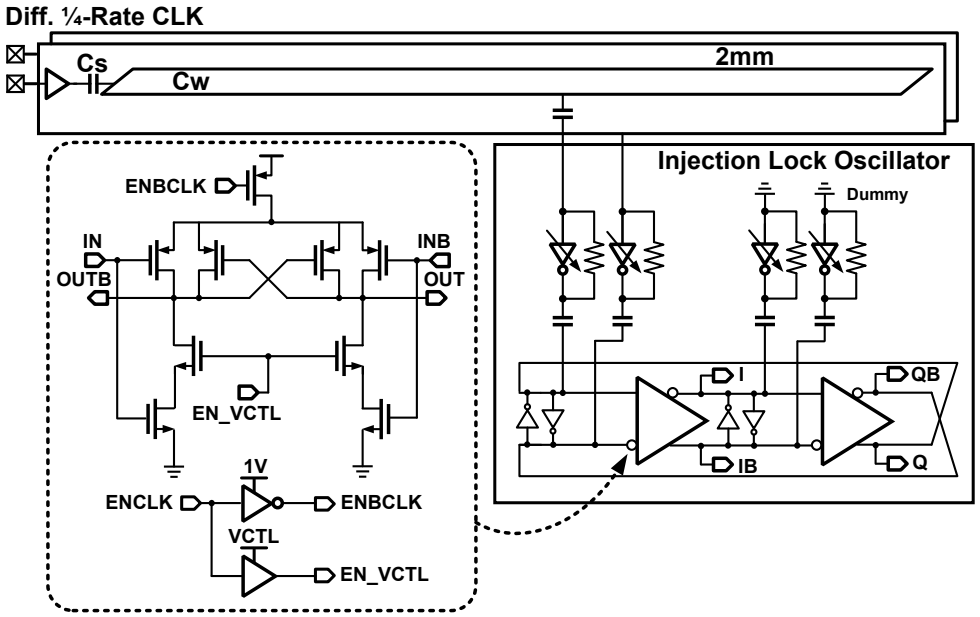


Multi-Channel TX Architecture

- Multi-channel transmitter architecture
  - Capacitive-driven global clock distribution
  - ILO-based multi-phase transmitter clock generation
- Scalable ¼-rate transmitter
  - Automatic phase calibration
  - Non-segmented impedance modulated equalization
  - Dual-supply replica-based voltage regulator

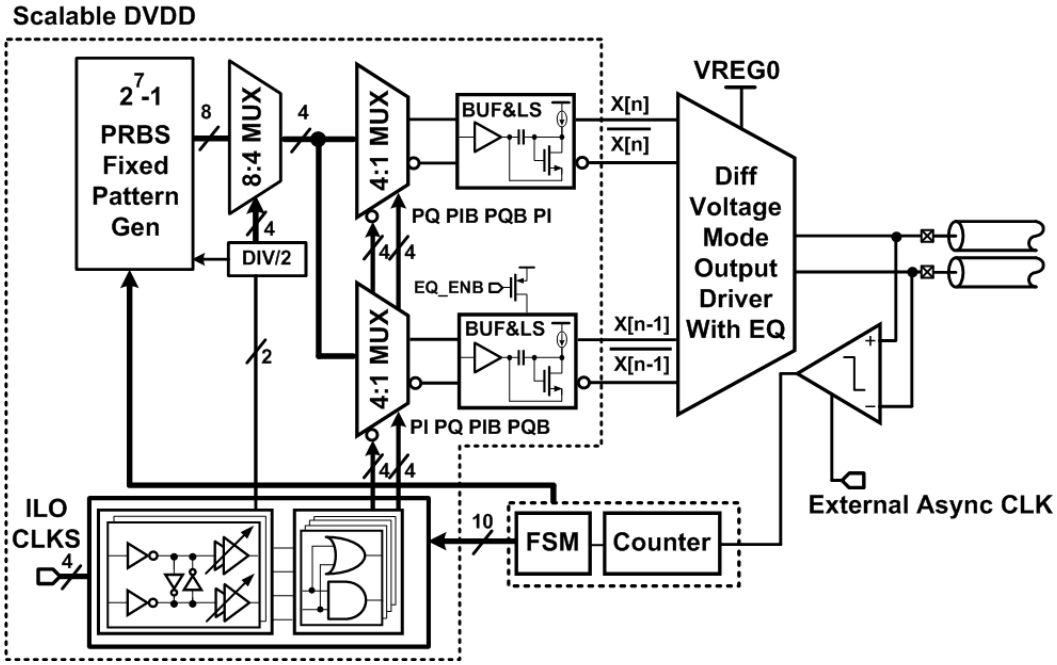


Transmitter Clocking



- Repeater-less capacitive-driven global clock distribution
  - Low swing and ¼-rate clock distribution
- 4-phase CLK generation by ILO
  - Eliminates low-to-high swing converter
  - Fine frequency control by EN_VCTL also enables fast power-state transitioning

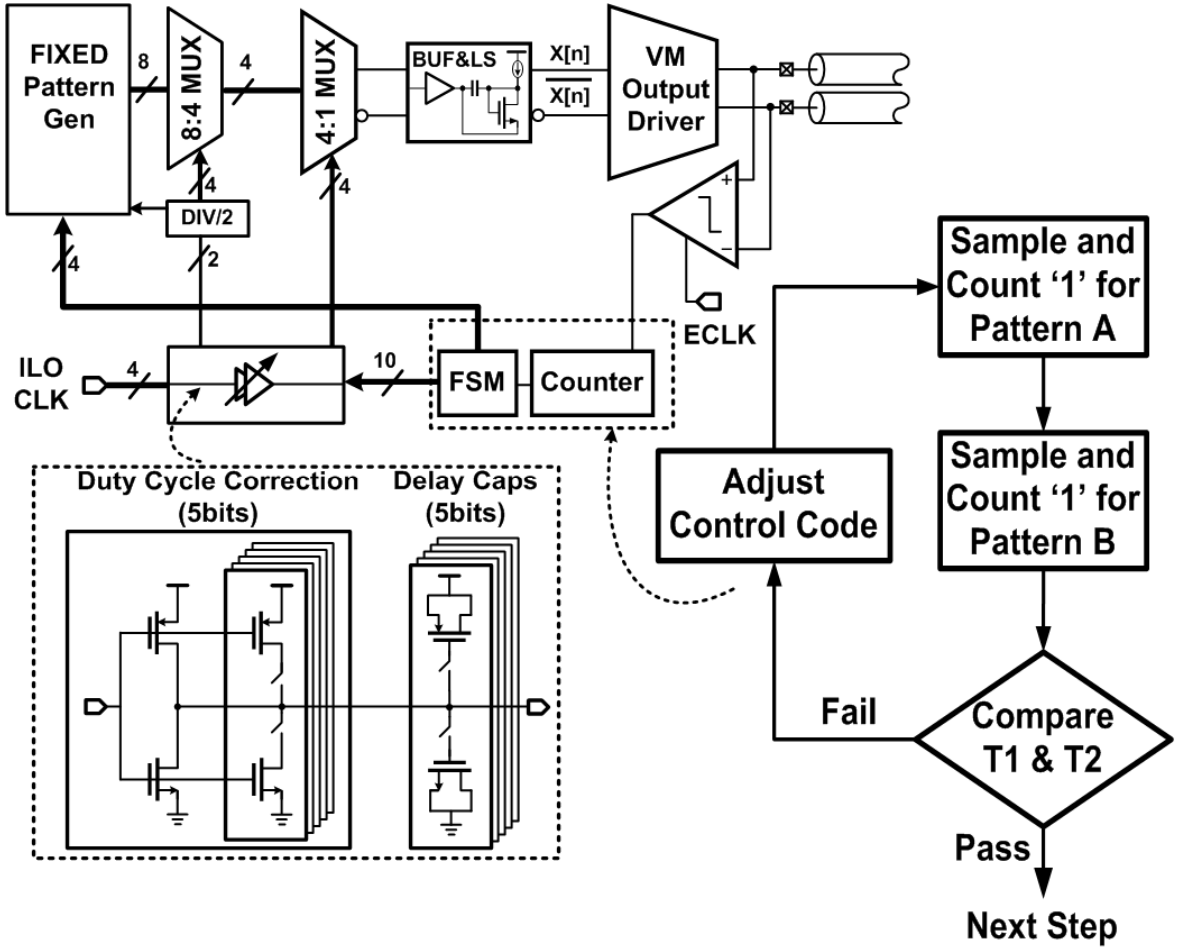
Transmitter Channel

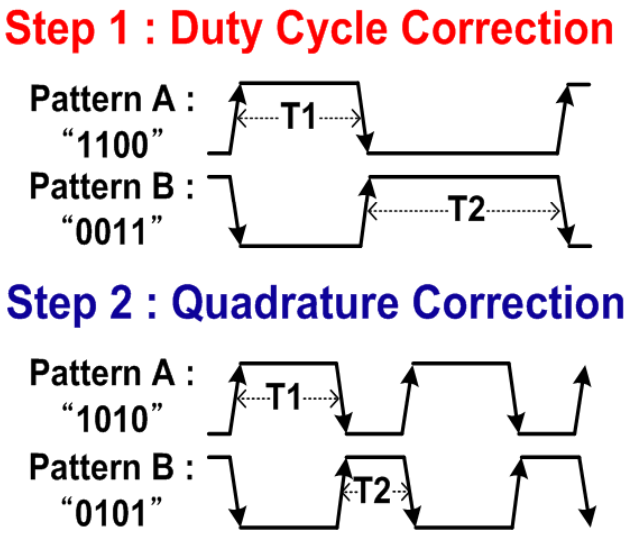


- Scalable quarter-rate transmitter
  - Supply scaling employed in data serialization and local clocking for optimal power at a given data rate
- 2-tap impedance modulated equalization
  - High-speed encoder eliminated due to analog tap control
- Automatic phase calibration for low-voltage operation

Async Sampling Based Phase Calibration

- Corrects for deterministic jitter caused by DCD and phase mismatches between quadrature clocks

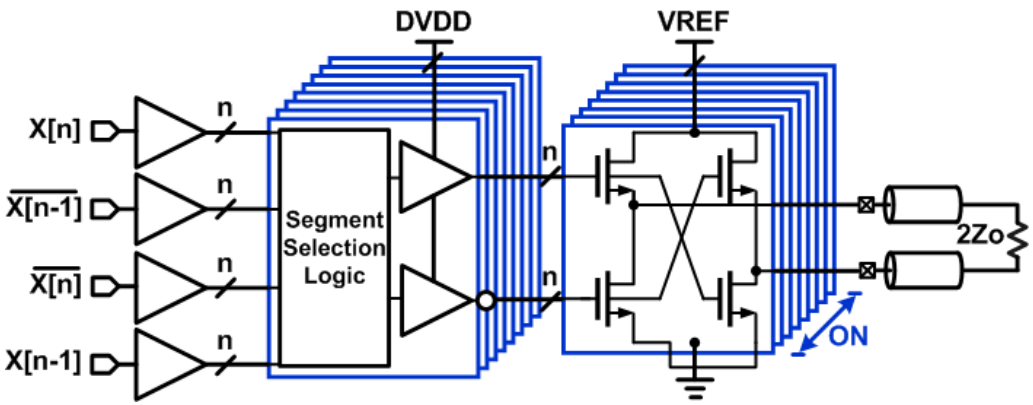


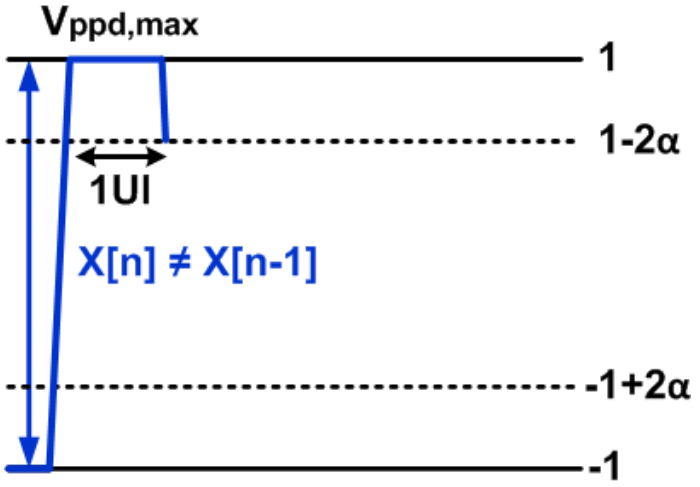


Impedance Modulated Equalization

- Signaling power reduces as de-emphasis increases
- Transition bits have 50Ω impedance
- Longer run length data has higher impedance

Segmented Implementation [2]





[2] R. Sredojevic, *et al*., JSSC 2011

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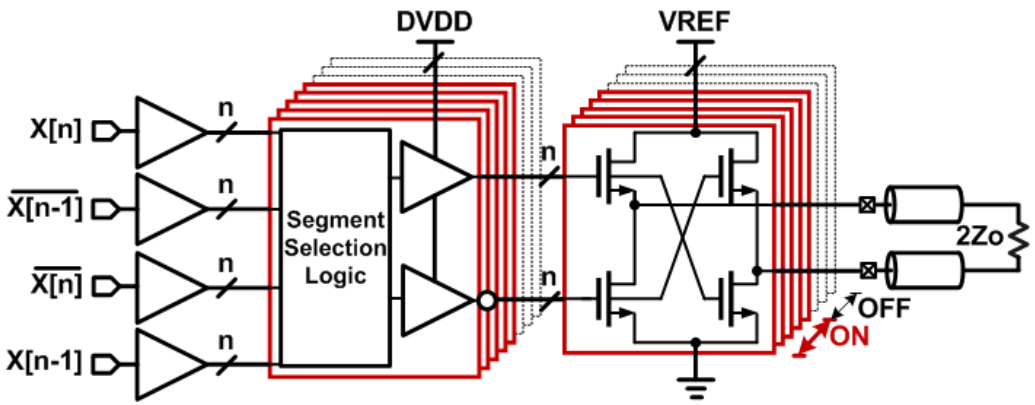
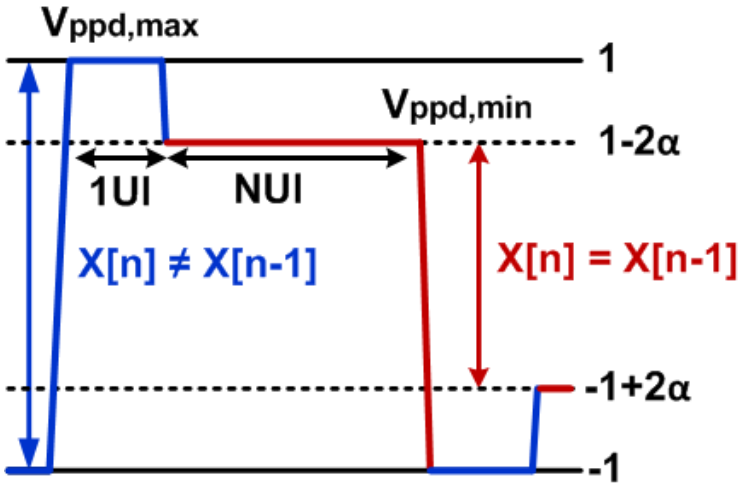
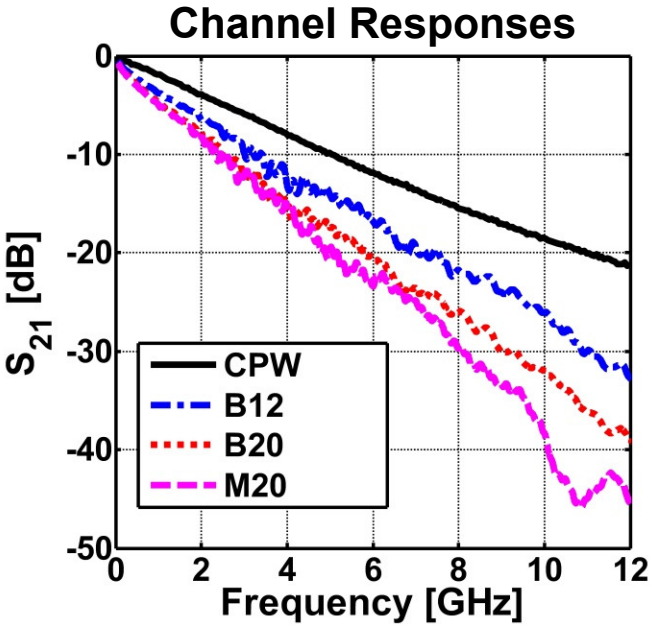


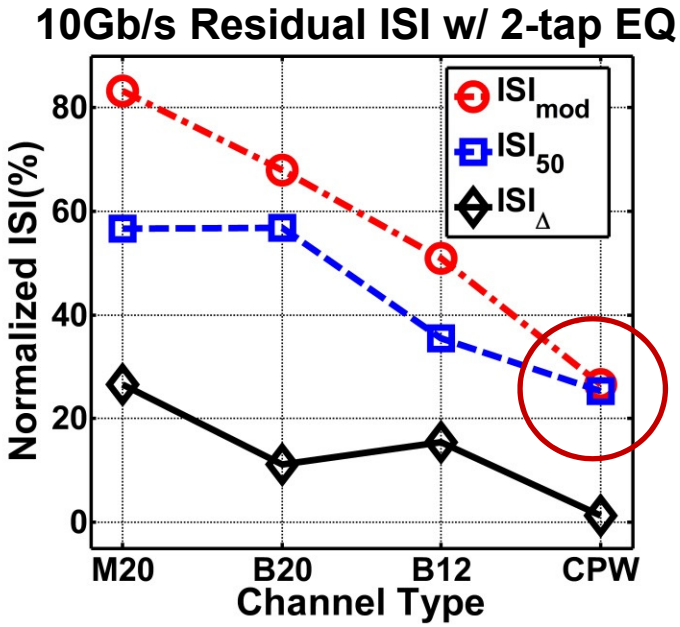


[2] R. Sredojevic, *et al.*, JSSC 2011

Relative Equalization Performance

- Relative equalization performance depends on the channel
- Channels with significant reflections (middle-trace backplane) can have >20% extra residual ISI
- Well-controlled impedance channels (single-board CPW) display almost identical performance

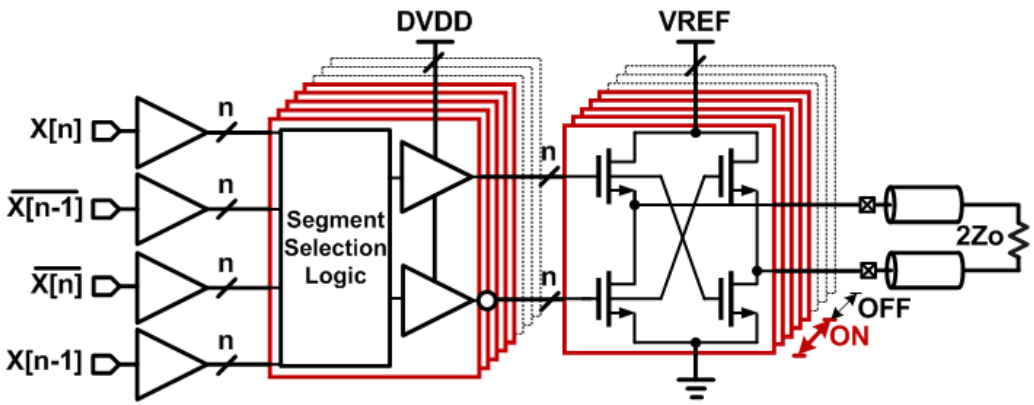




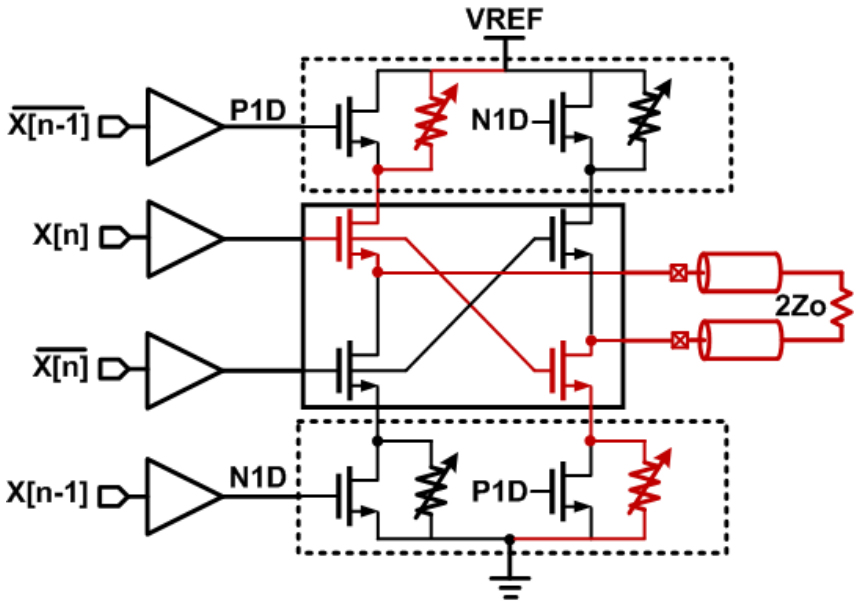
Equalization Tap Control

- Segmented pre-driver and output driver significantly increases dynamic power consumption with increased equalization resolution

Segmented Implementation [2]



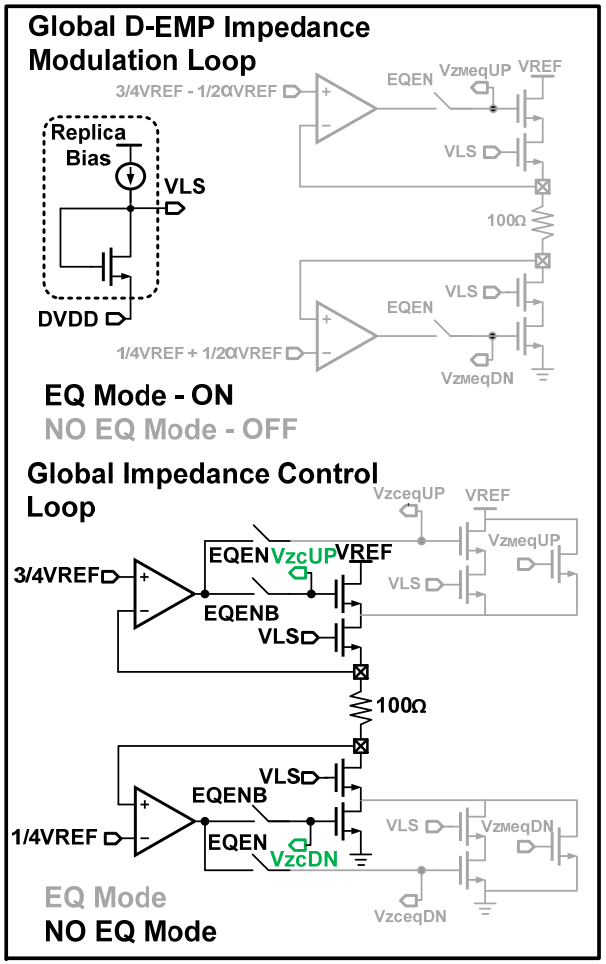
Proposed non-segmented Implementation

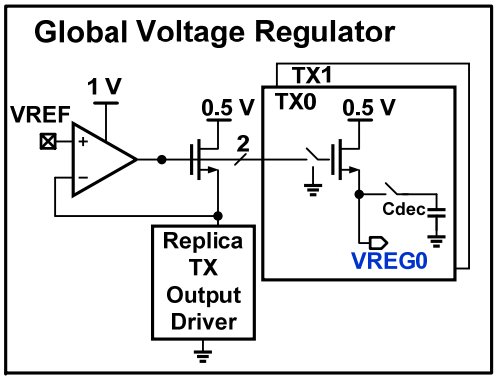


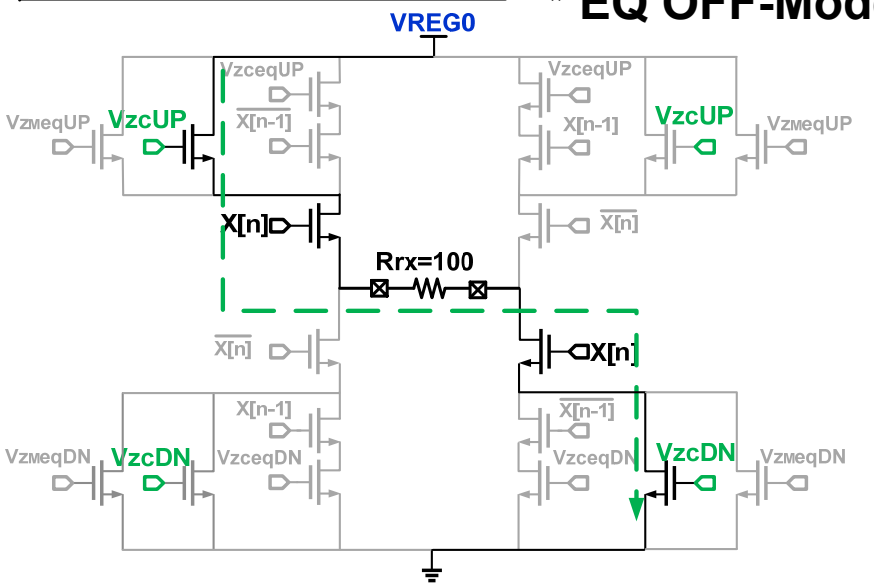
[2] R. Sredojevic, *et al.*, JSSC 2011

TX Output Driver w/Analog Control

- Global impedance modulation/control loops and voltage regulator allows for power amortization

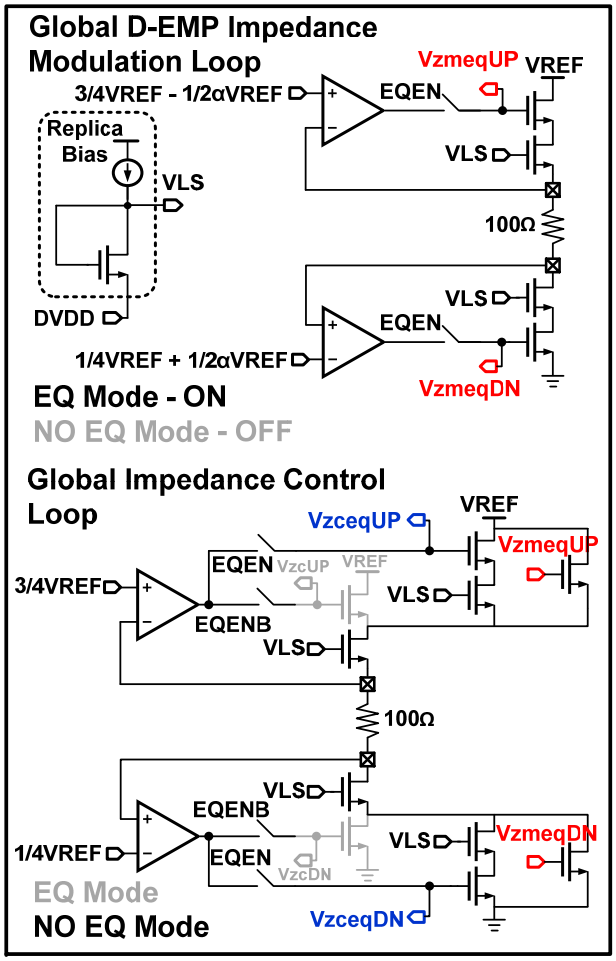


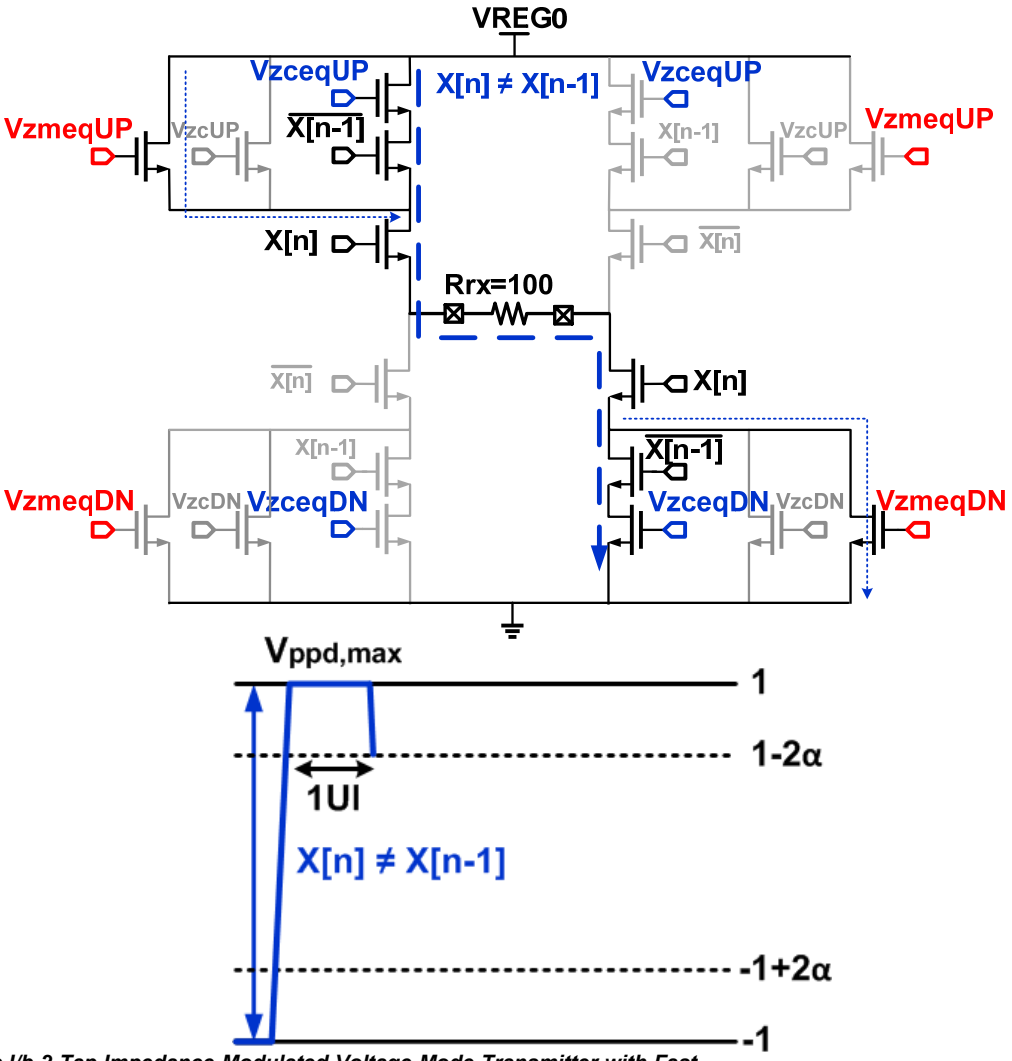




Impedance Modulated EQ Mode

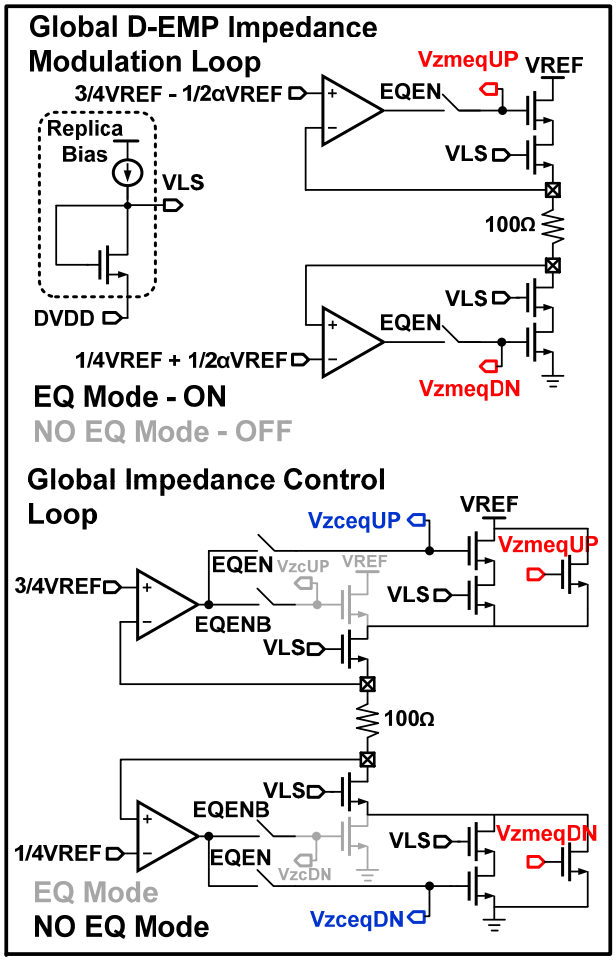
- Maximum transmitter output swing during a transition bit

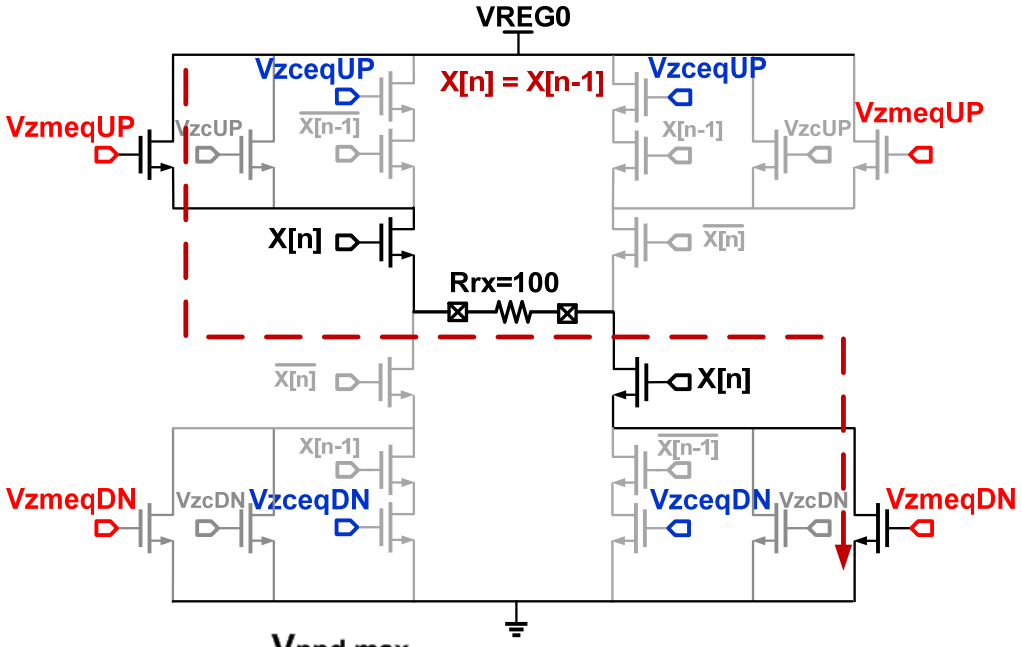


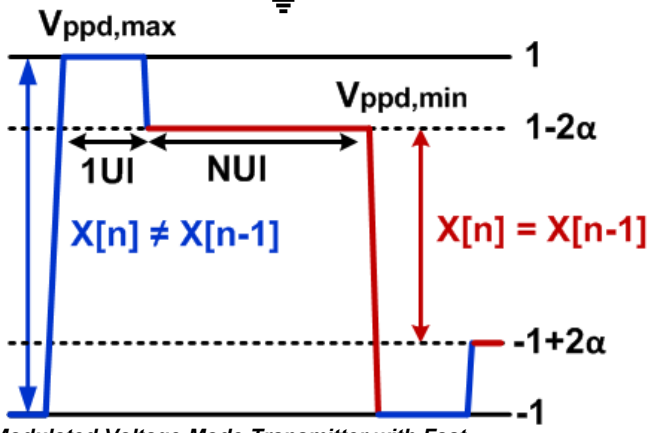


Impedance Modulated EQ Mode

- De-emphasis transmitter output swing (Analog control) for run-length > 1

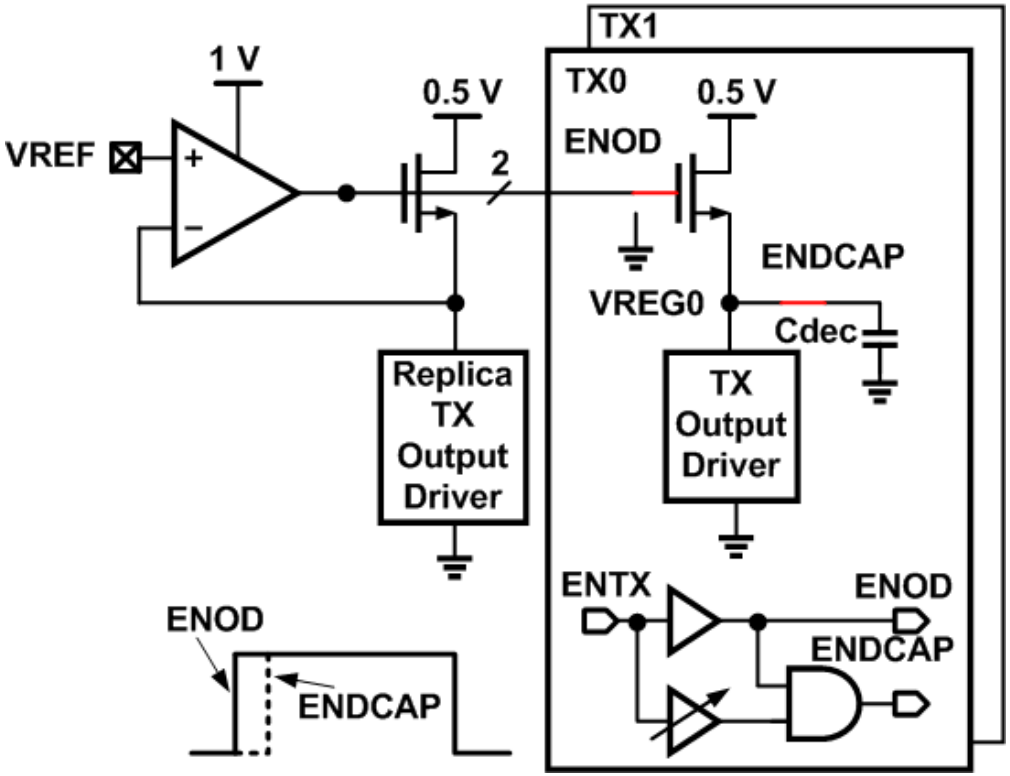


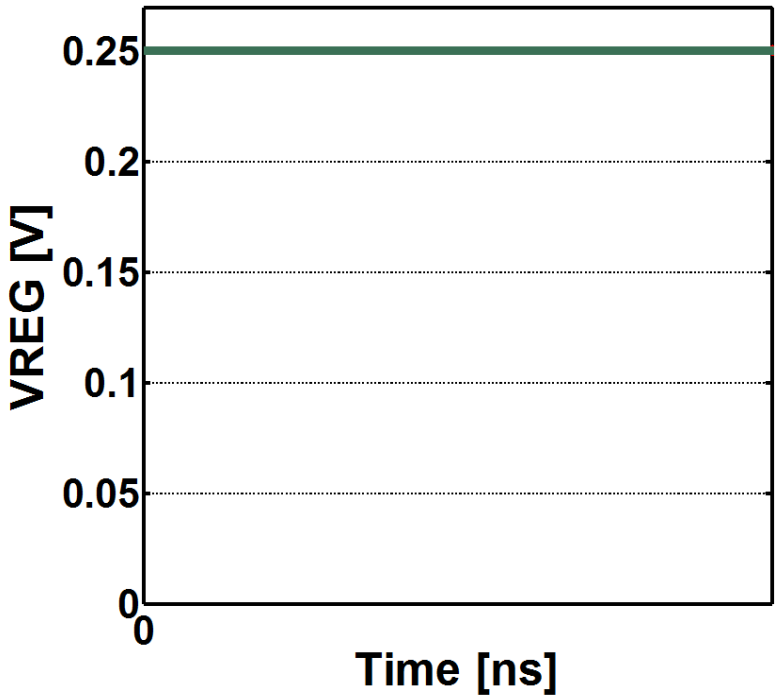




Replica-Biased Voltage Regulator

- Dual supply implementation allows for improved error amp accuracy and lower output stage power
- Fast power state transition time enabled with bias switching and staggered enabling of output decoupling capacitance





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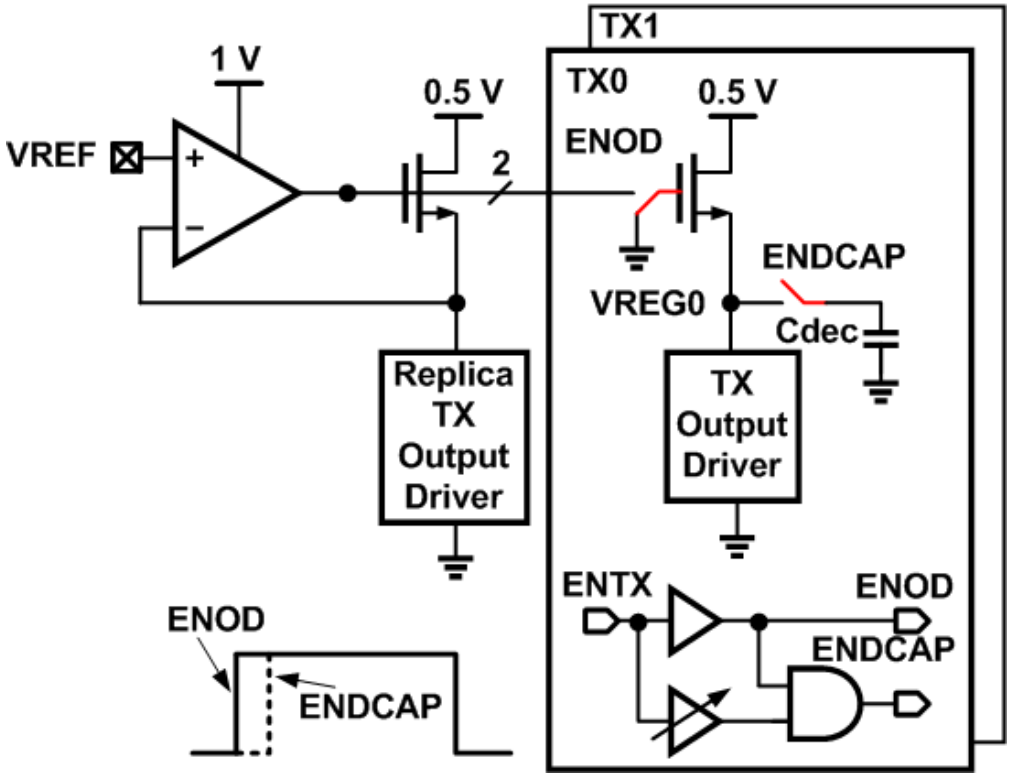

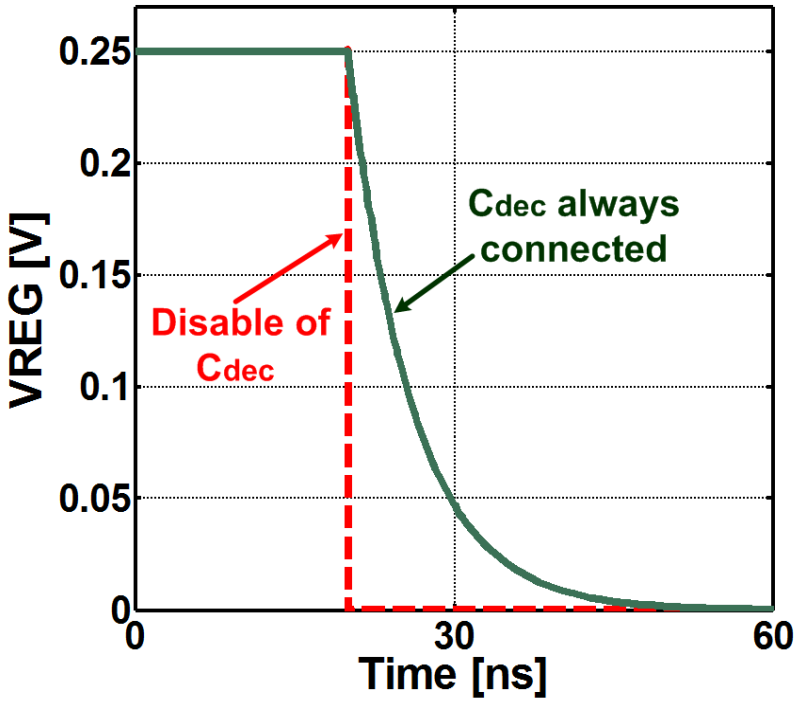

Replica-Biased Voltage Regulator

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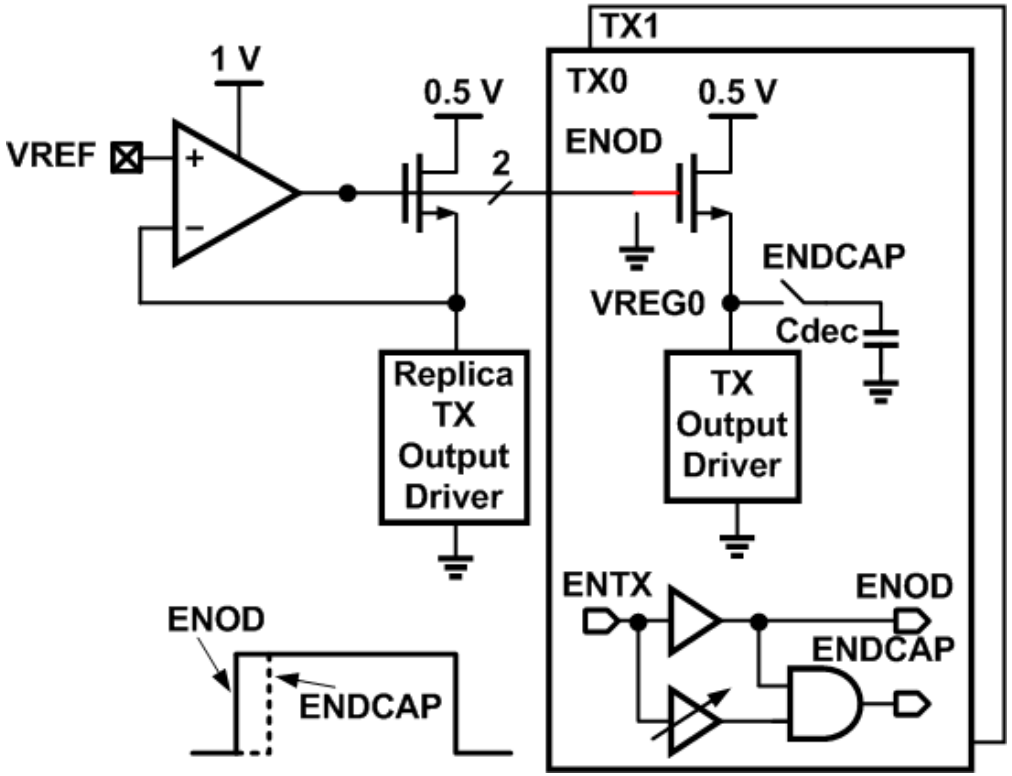
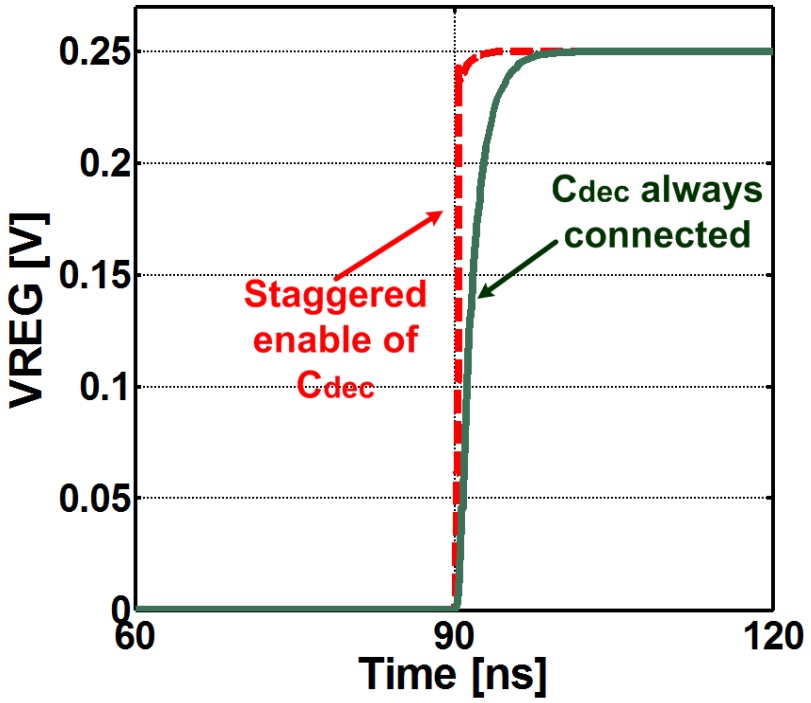
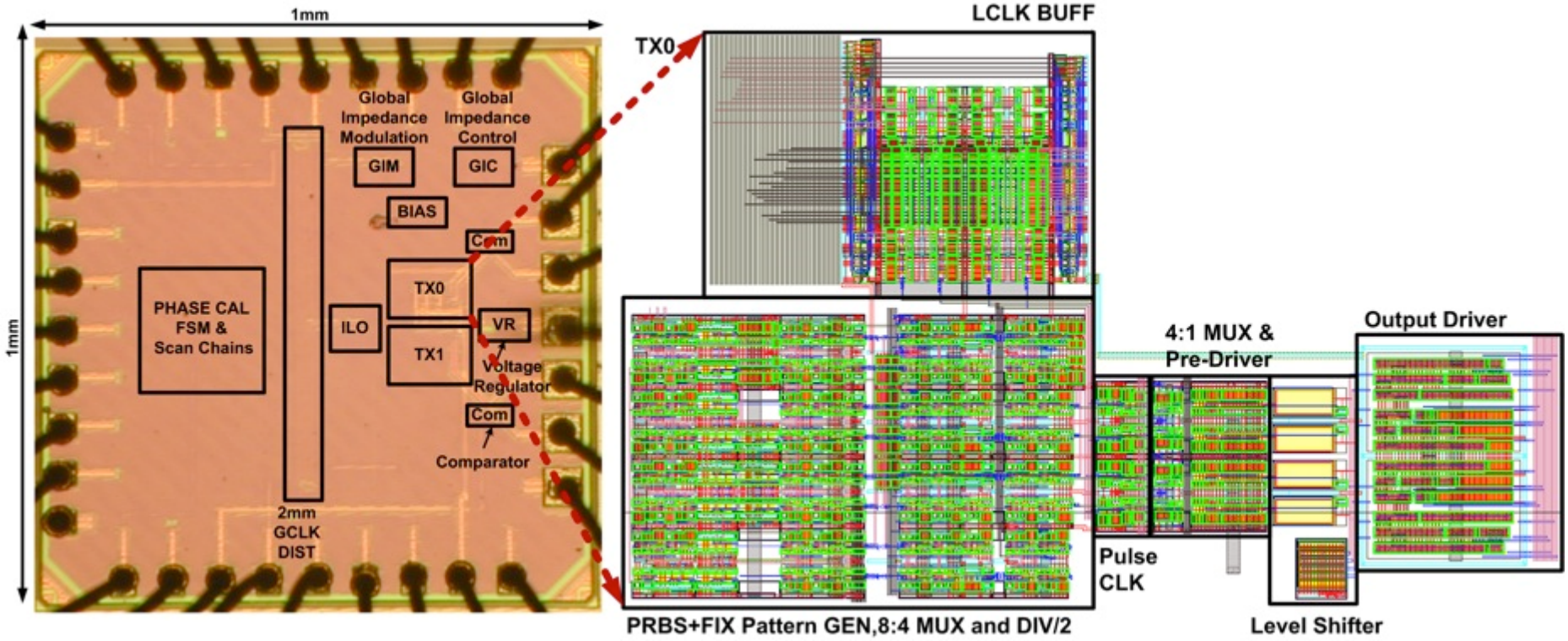


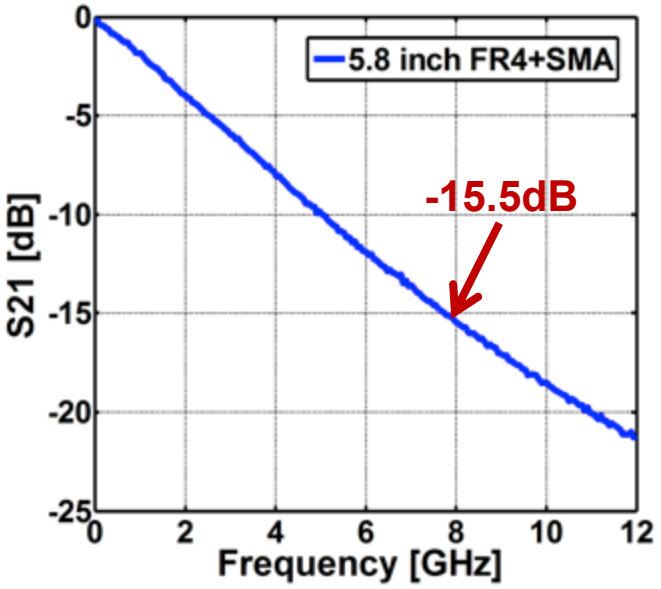


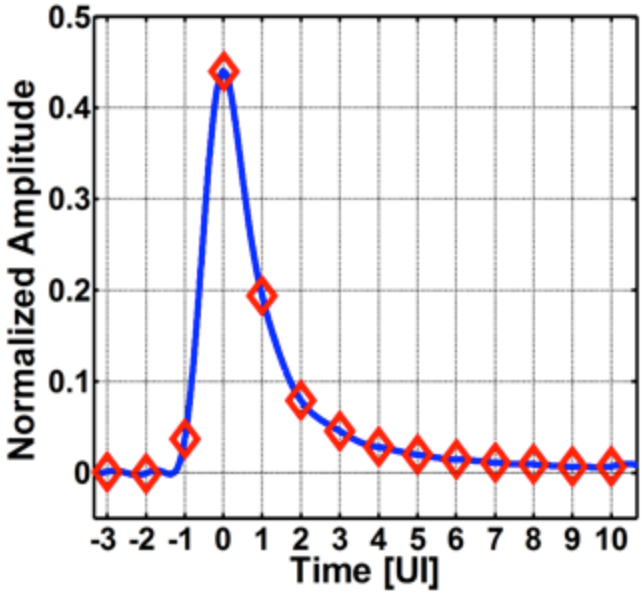
GP 65nm CMOS Prototype

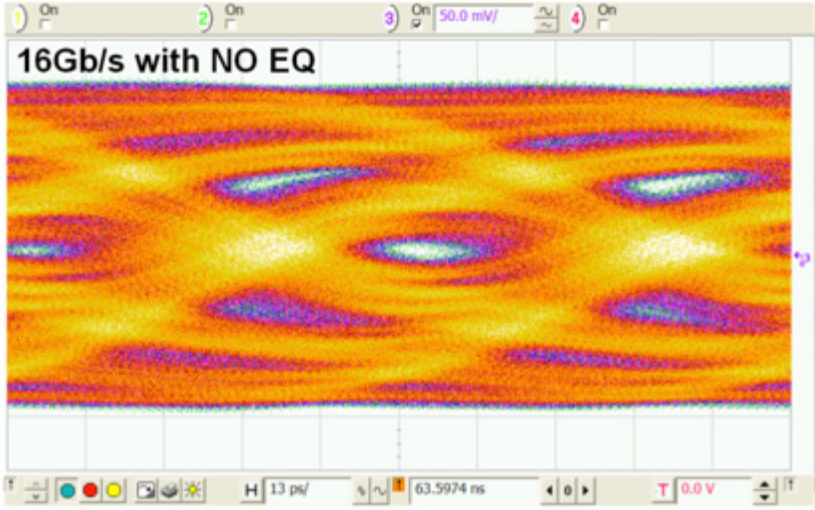
TRANSMITTER ACTIVE AREA							
TX0	PRBS+8:4MUX DIV/2	Local CLK Buffer	Pulse CLK	4:1MUX & Pre-Driver	Level Shifter	Output Driver	Total
Active Area	41umX65um	35.2umX54um	21.6umX7.5um	21.6umX16um	31umX12um	32umX29um	0.006mm^2

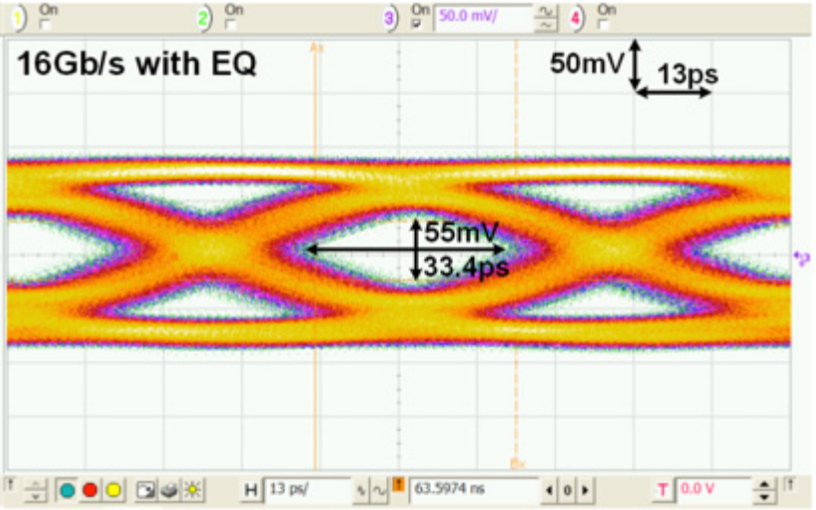


16Gb/s Operation



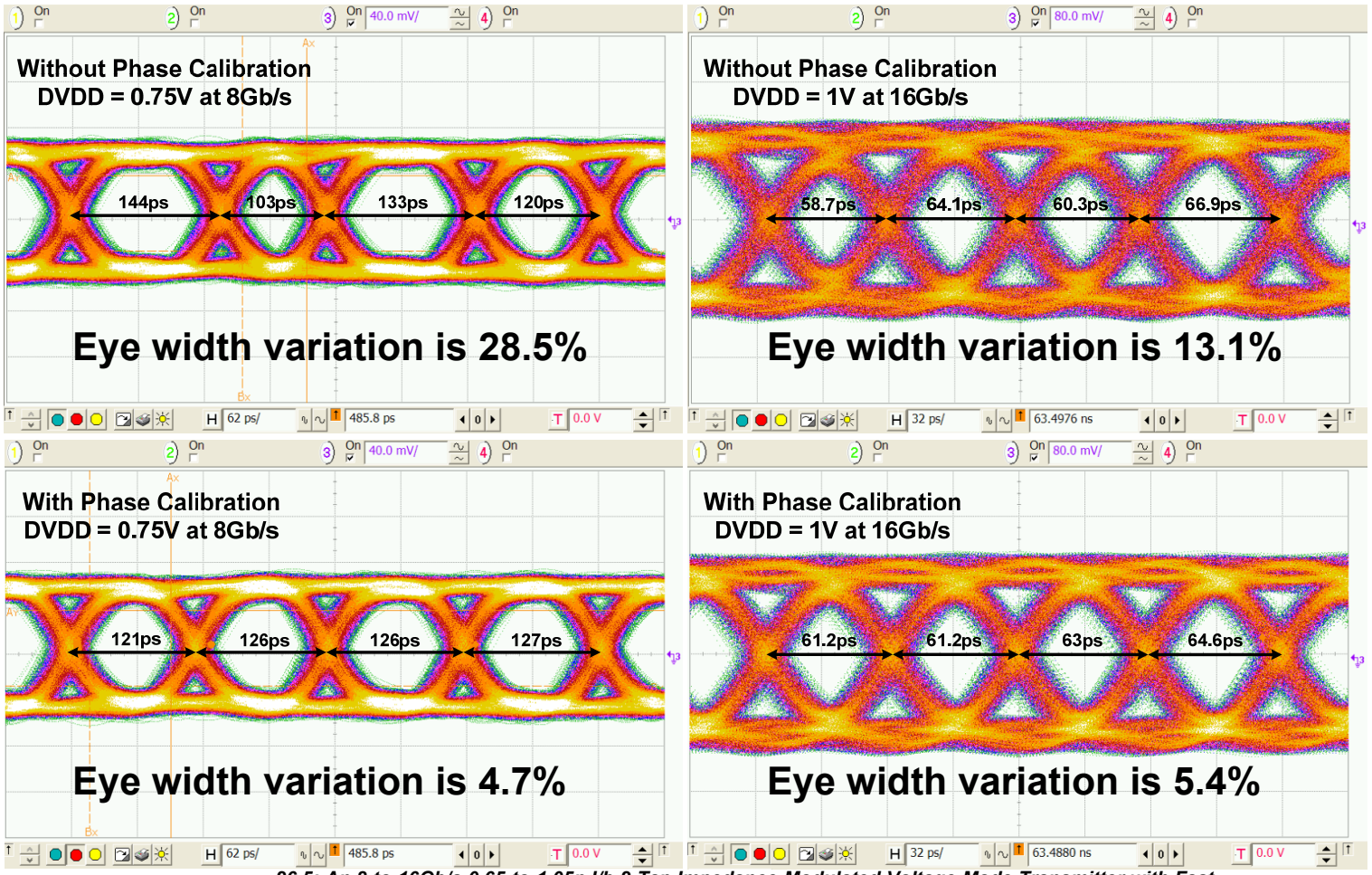






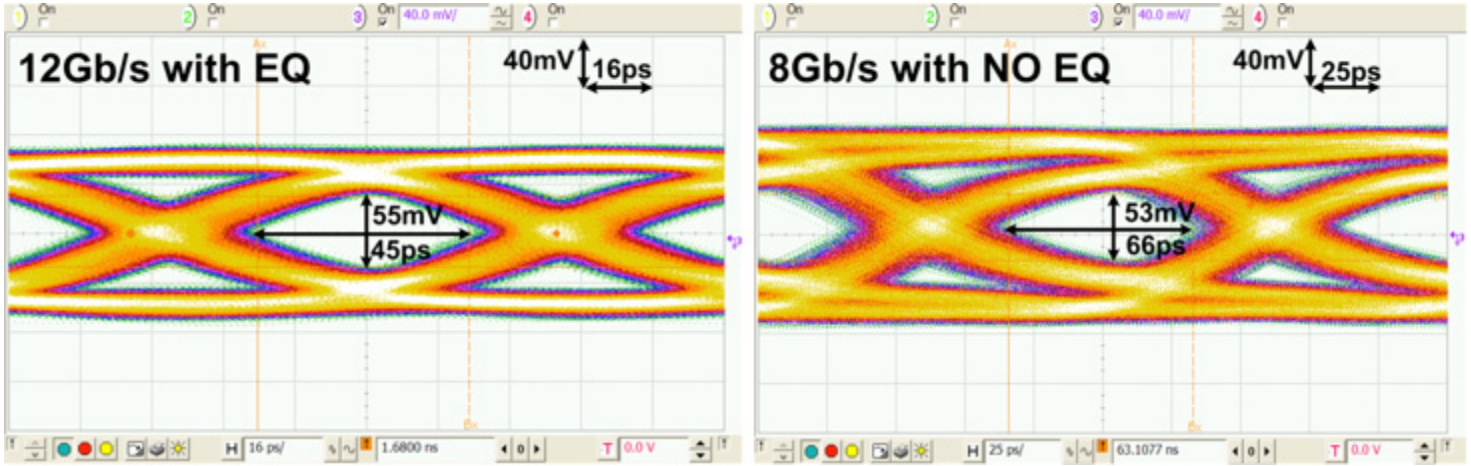
Automatic Phase Correction

- Eye diagrams without and with phase calibration after 2” FR4

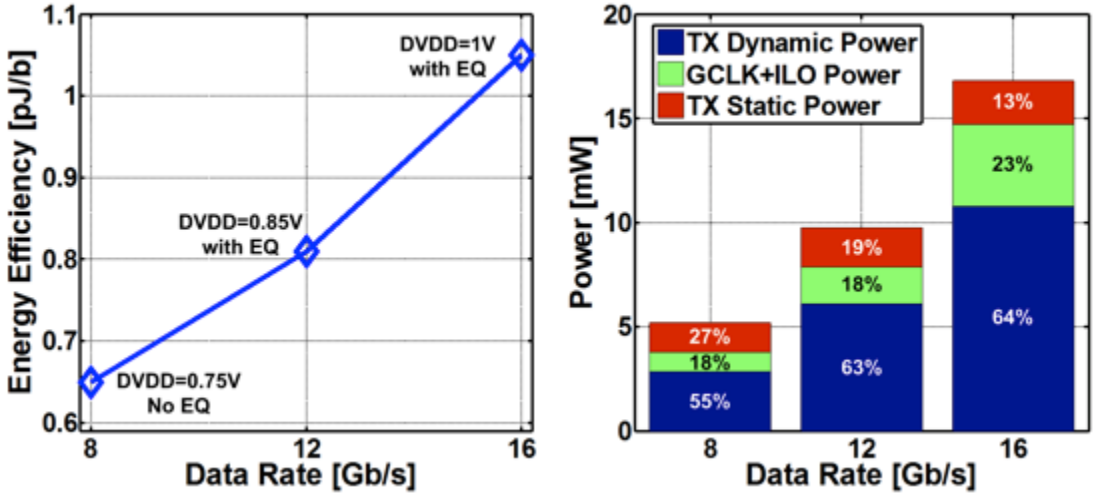


Energy Efficiency Scaling

- Equalization enabled for 12Gb/s and disabled at 8Gb/s

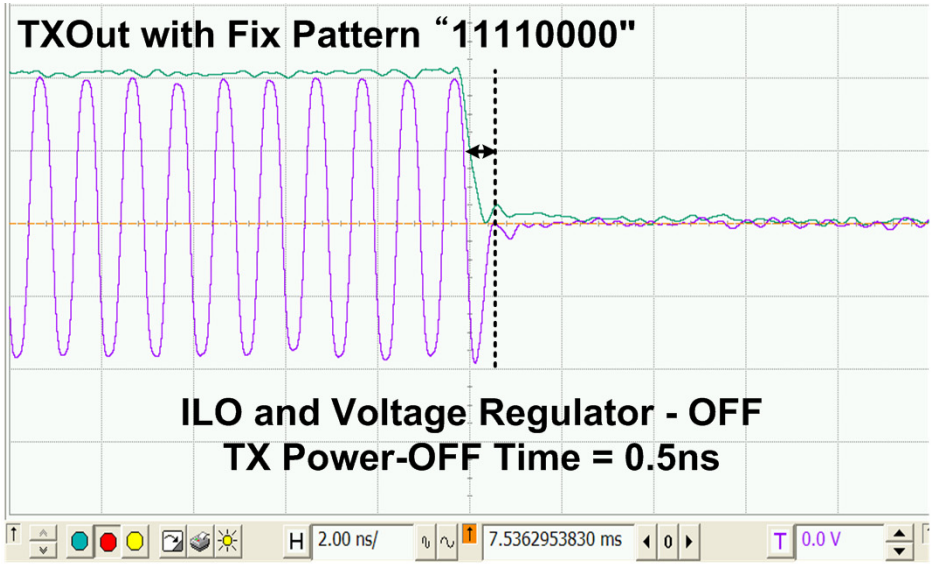


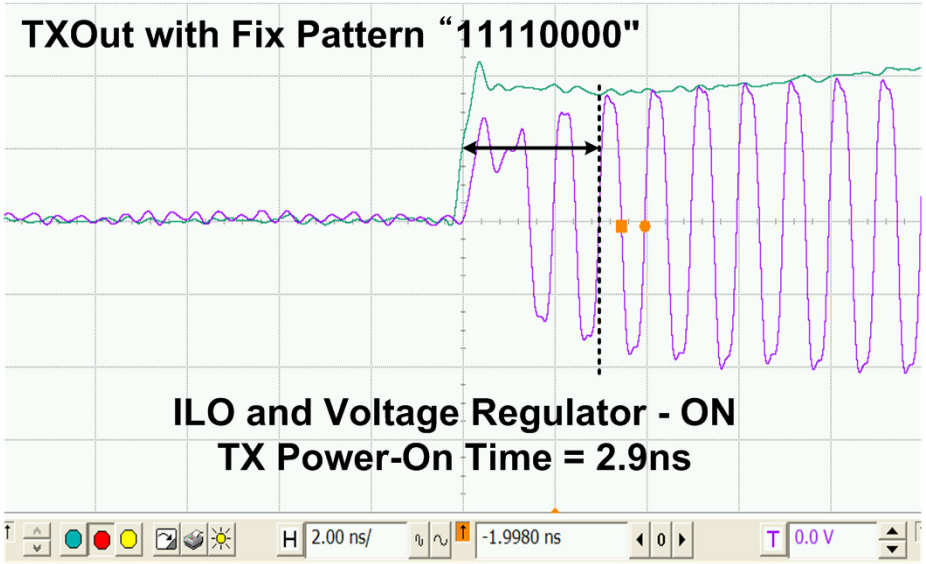
- Energy efficiency and power breakdown for 50mV$_{ppd}$ & 0.5UI



Fast Power-State Transitioning

- Transmitter output under fast power-down and start-up





[4] B. Leibowitz, *et al* JSSC 2011
[5] J. Zerbe, *et al* VLSI 2011
[6] F. O'Mahony, *et al* ISSCC 2010

POWER STATE TRANSIENT TIME COMPARISONS				
	[4]	[5]	[6]	This Work
Technology	40nm	40nm	45nm	65nm
Data Rate	4.3Gb/s	5.6Gb/s	10Gb/s	16Gb/s
Power State Transient time	**<5ns**	**8ns**	**<5ns**	**0.5ns(Off), 2.9ns(On)**

Performance Summary

TRANSMITTER POWER BREAKDOWN (16Gb/s at 1V & 0.5V)	
LDO (amortized across 2 TX) & Output Driver (300mV$_{ppd}$ with EQ)	985uW
Serializer, Pre-drivers, Clocking	10.8mW
Global Impedance Control & Modulation Loop, Bias Circuit (amortized across 2 TX)	1.1mW
Global Clocking (amortized across 2 TX)	1.5mW
ILO (amortized across 2 TX)	2.4mW
Total Energy Efficiency	**1.05pJ/b**

TRANSMITTER PERFORMANCE COMPARISONS			
	[2]	[3]	This Work
Technology	90nm	65nm	65nm
Supply Voltage	1.15V	1.2V	1 & 0.5V
Data Rate	4Gb/s	10Gb/s	**16Gb/s**
TX Swing	0V-1Vppd	160mV~ 500mVppd	100mV~ 300mVppd
Channel Loss @ Nyqu. Freq	-8~-10dB	-13dB	**-15.5dB**
Equalization	2-Tap FIR	2-Tap FIR	2-Tap FIR
Energy Efficiency	**1.25-4.25pJ/b**	**1pJ/b**	**1.05pJ/b**

[2] R. Sredojevic, *et al*., JSSC 2011
[3] Yue Lu, *et al*., JSSC 2013

Conclusion

- Presented 2-tap analog impedance modulated equalization transmitter achieves 8-16Gb/s with 0.65pJ/b-1.05pJ/b
- Low swing quarter-rate capacitive-driven global clock distribution with ILO reduces global clocking power
- Automatic phase calibration allows for aggressive reductions in supply voltage
- Fast power-state transitioning enabled with a replica-biased voltage regulator and ILO local clocking

Acknowledgements

This work was supported in part by the Semiconductor Research Corporation (SRC) under Task 1836.060 through the Texas Analog Center of Excellence (TxACE), the Intel Wireline Signaling Program, and a Department of Energy Early Career grant.

A 2.667 Gb/s DDR3 Memory Interface with Asymmetric ODT on Wirebond Package and Single-Side Mounted PCB

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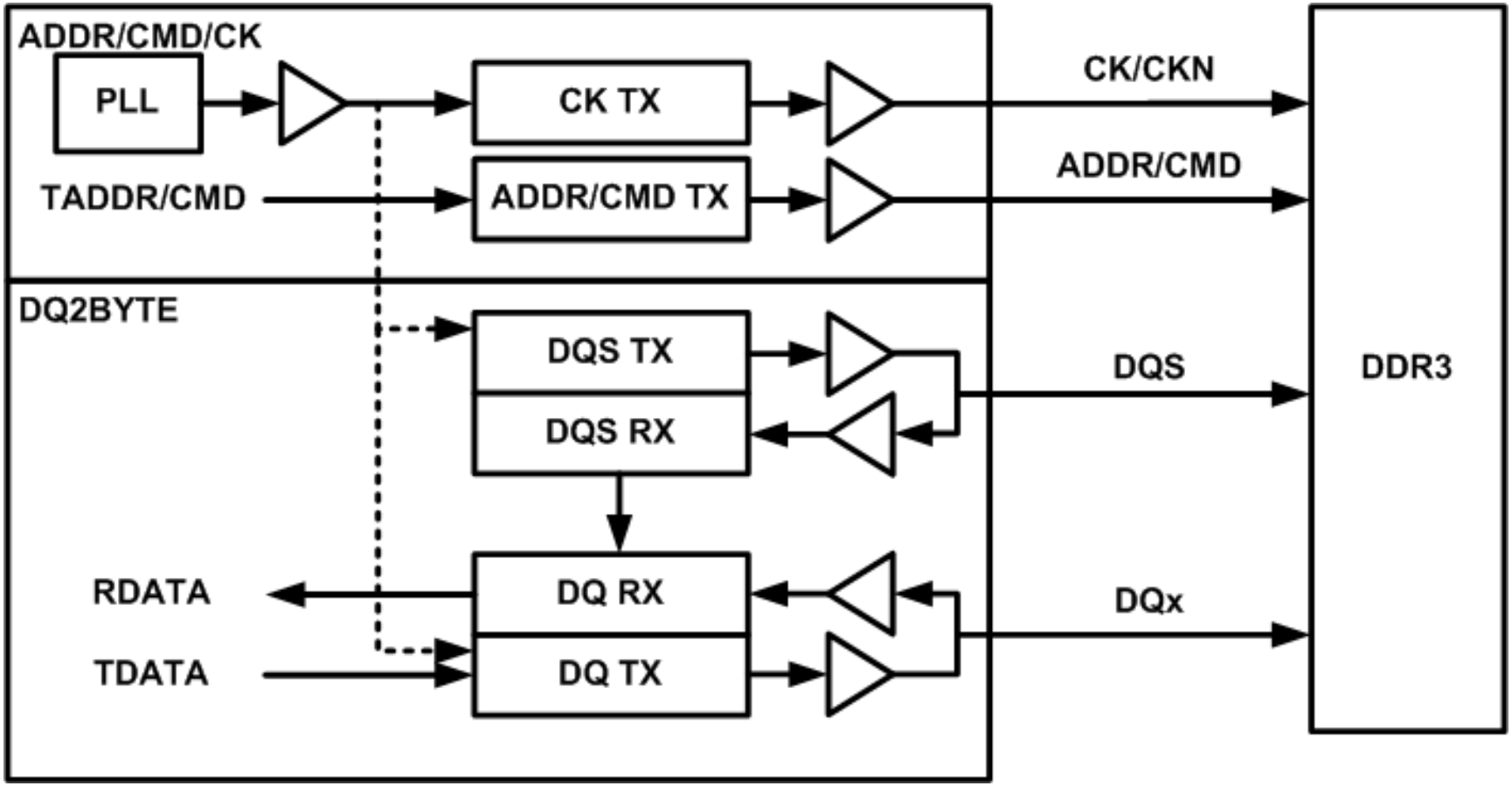
MediaTek, Hsinchu,Taiwan

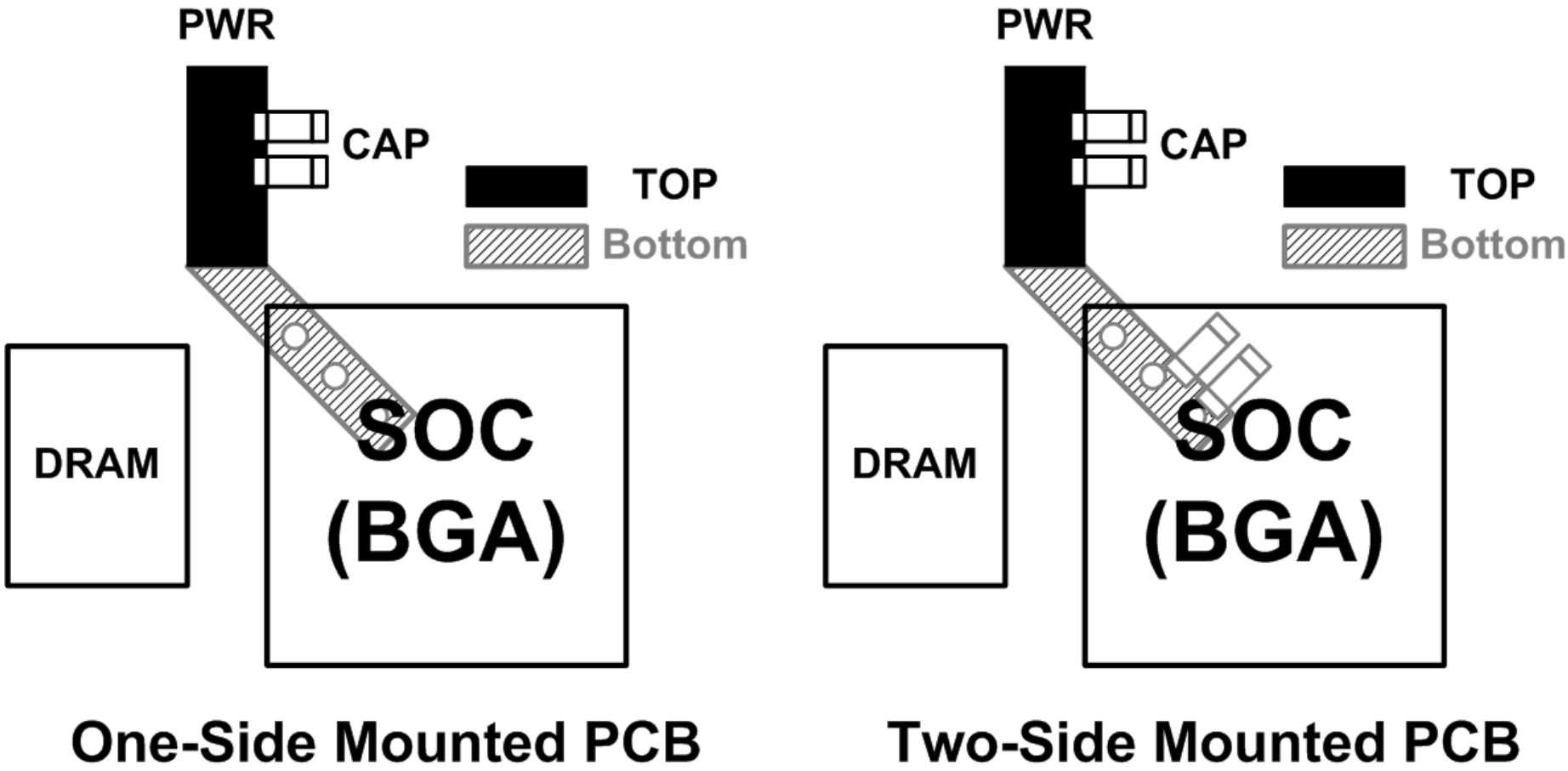
Outline

- Motivation
  - Memory interface overview
  - One-side mounted PCB
- Developed Memory interface
  - Output stage with clock base LS
  - Input stage with asymmetric ODT
  - Termination topology.
- Measurements
- Summary

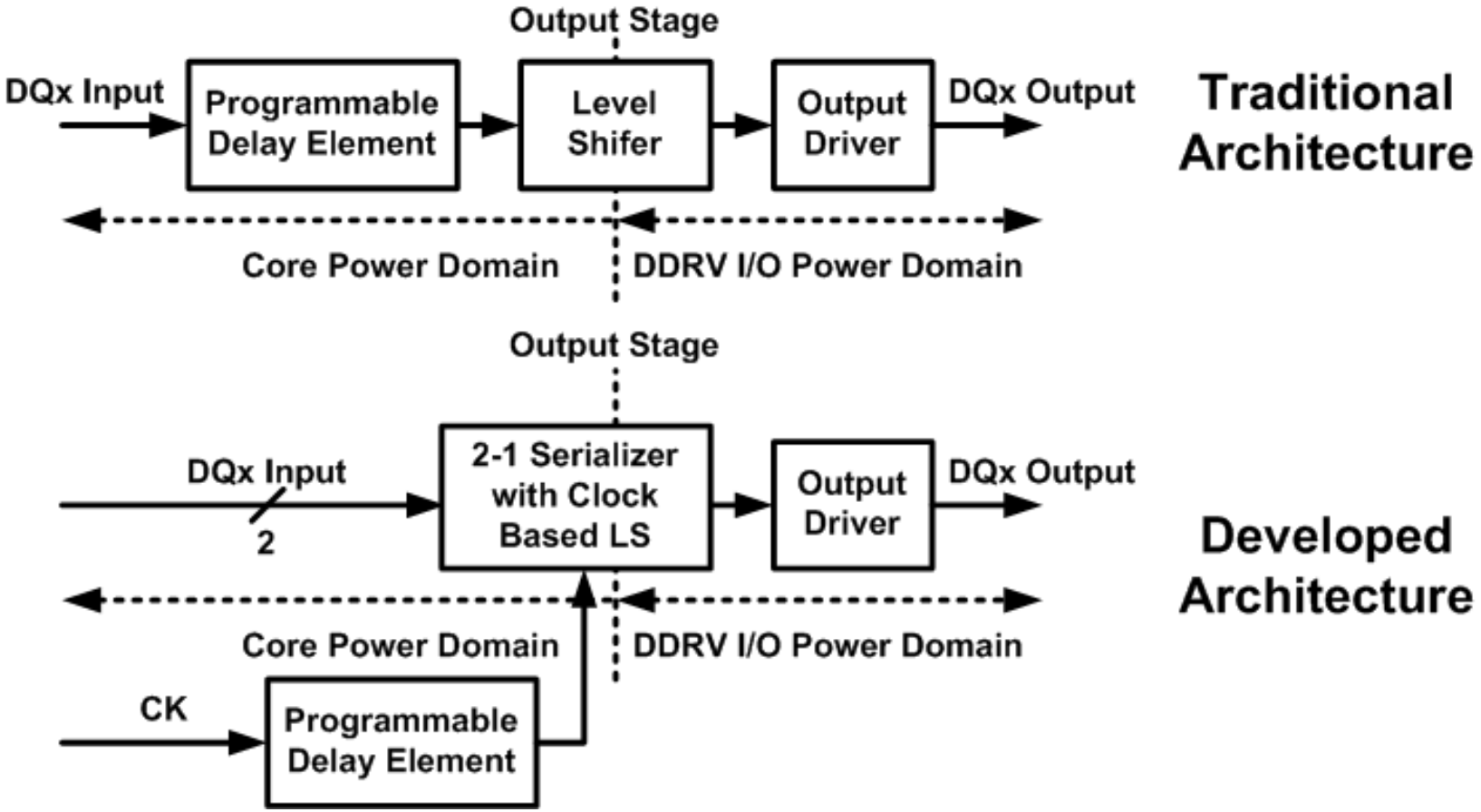
Memory interface system



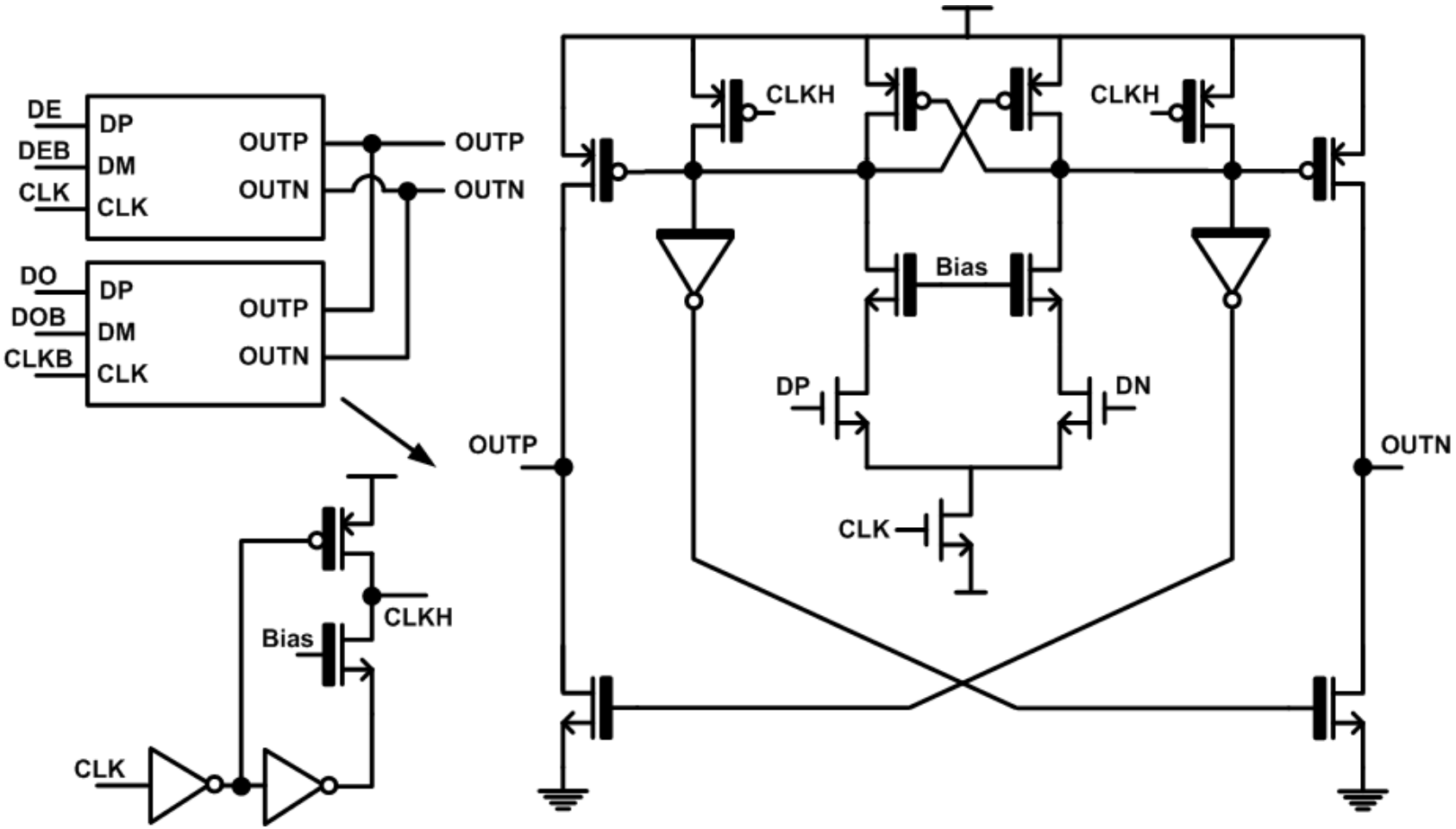
One-side Mounted PCB



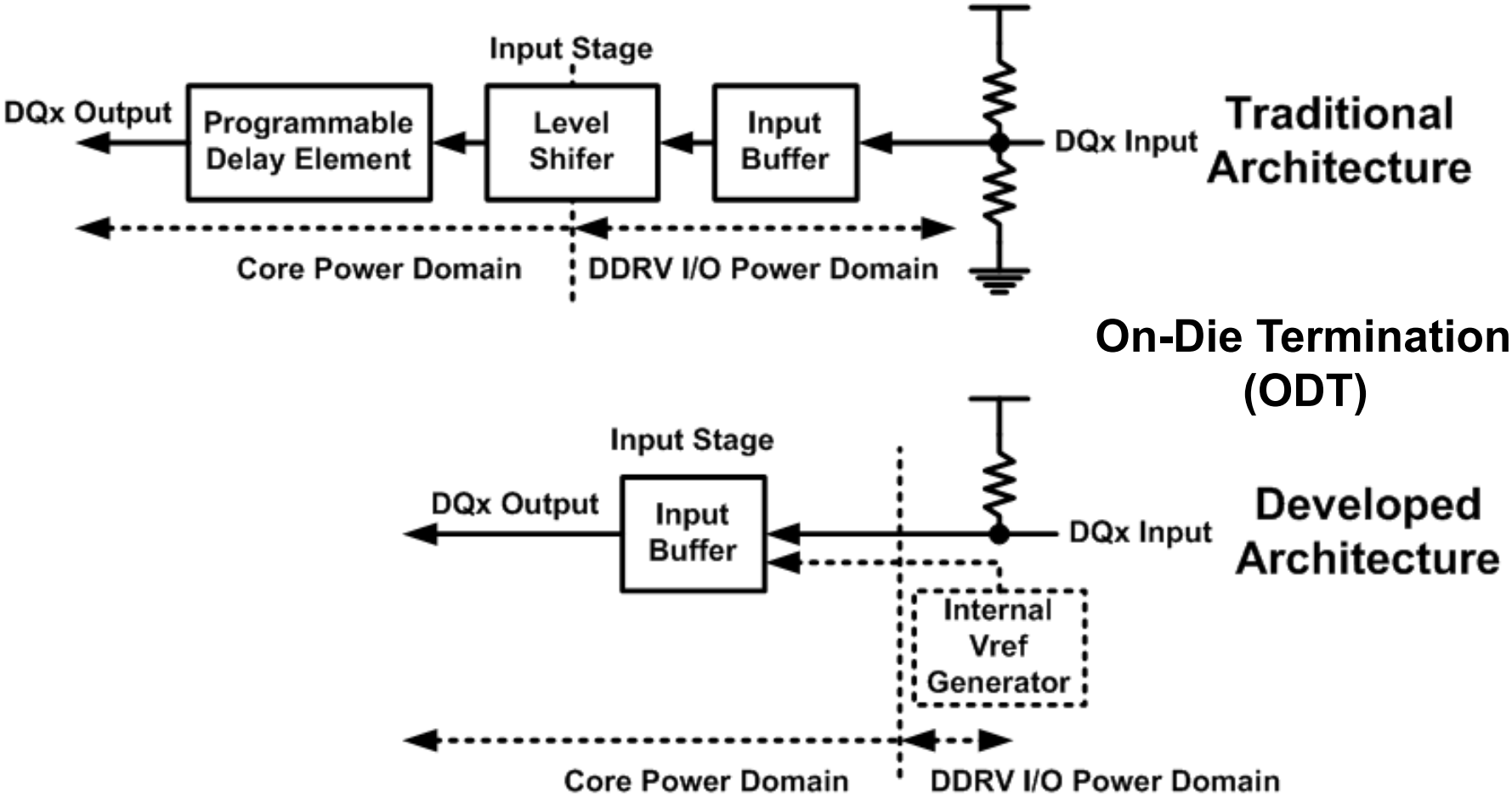
Developed Memory Output Stage



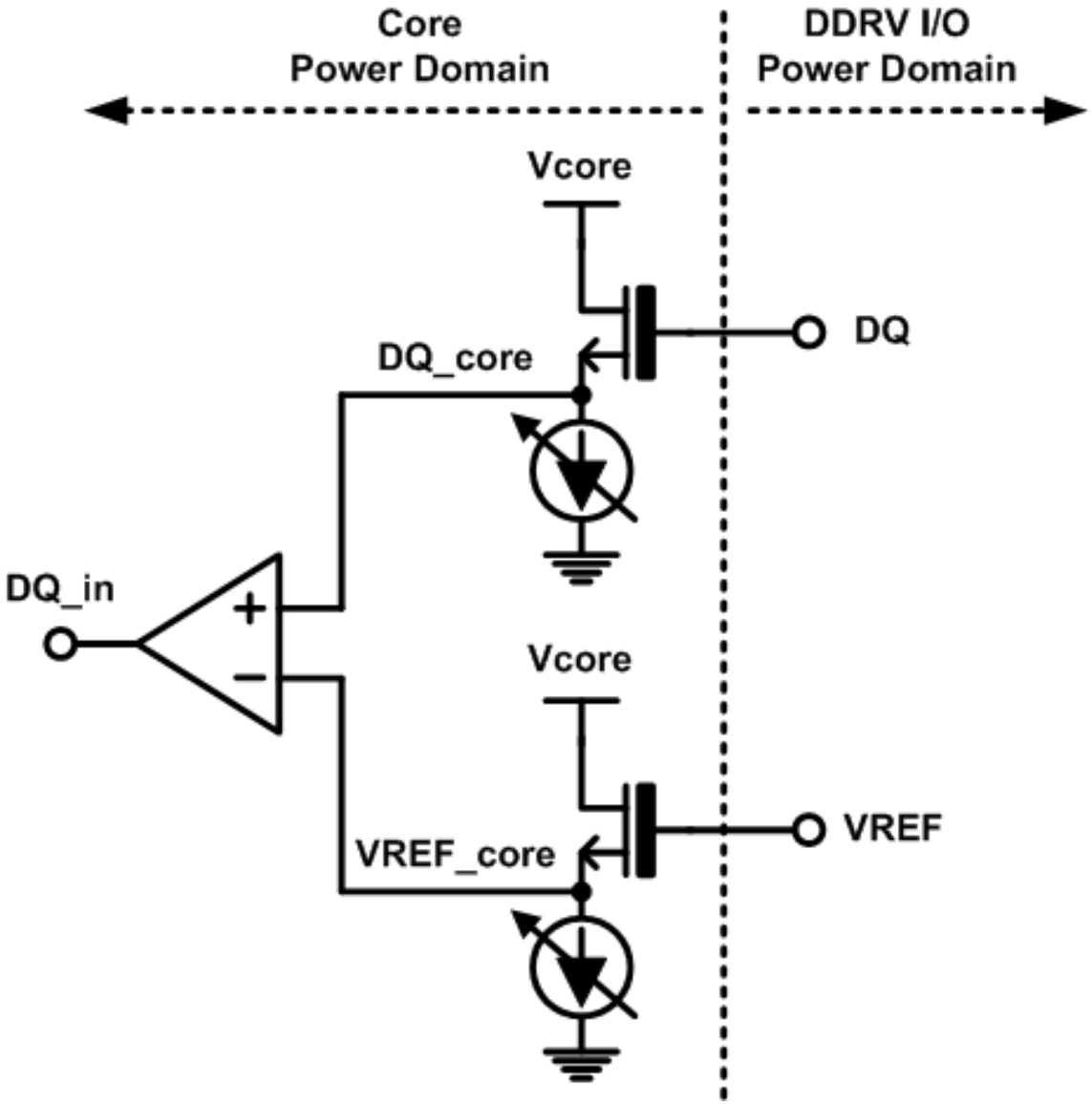
2-to-1 Serializer w/i Clock Based LS



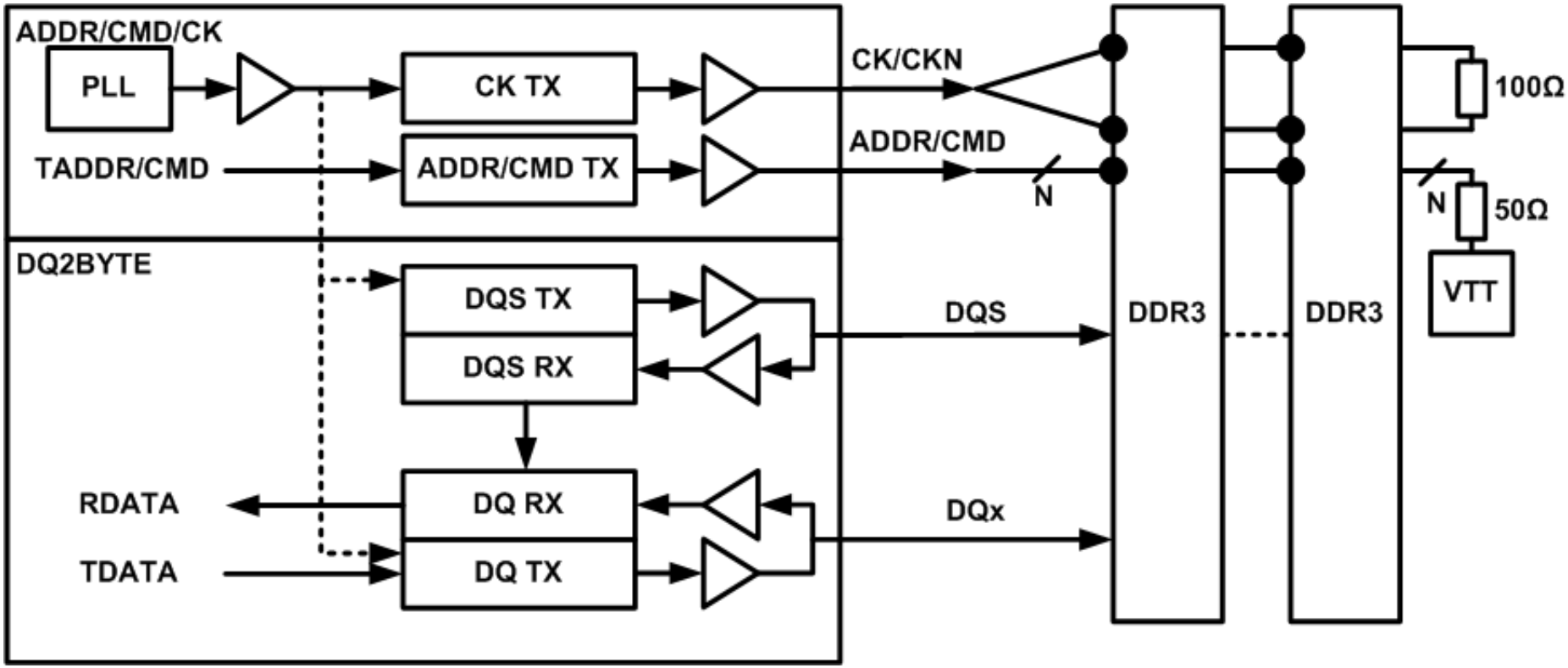
Developed Memory Input Stage



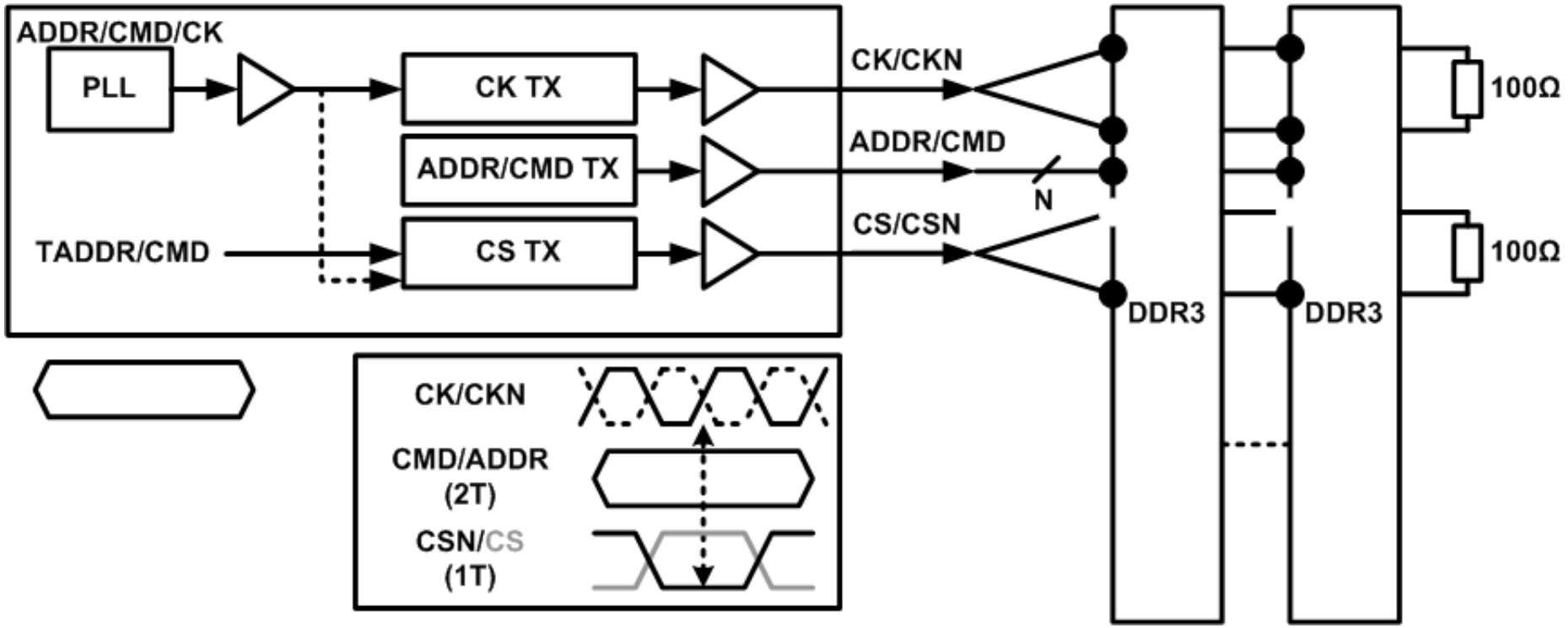
Input Buffer



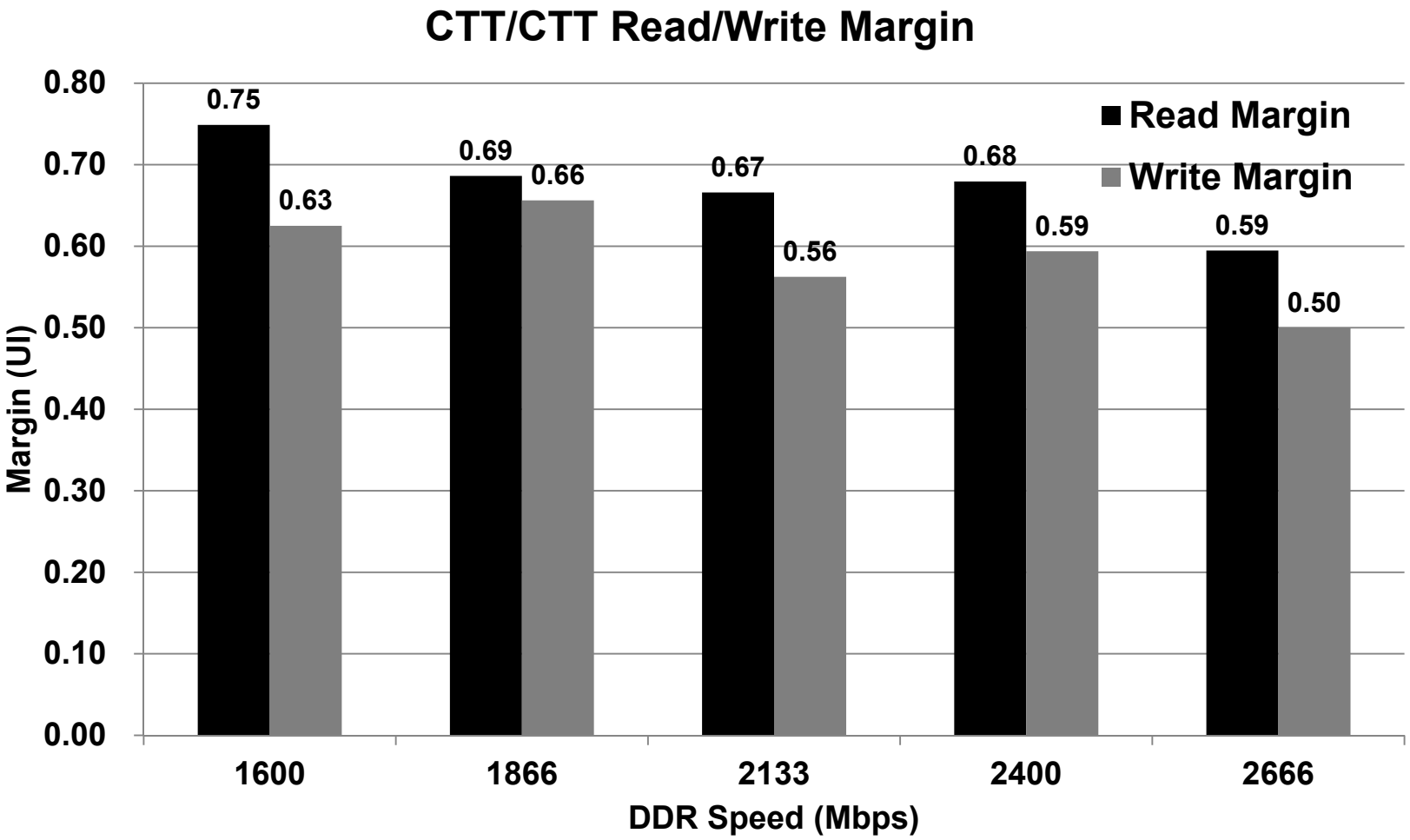
Fly-by Termination topology



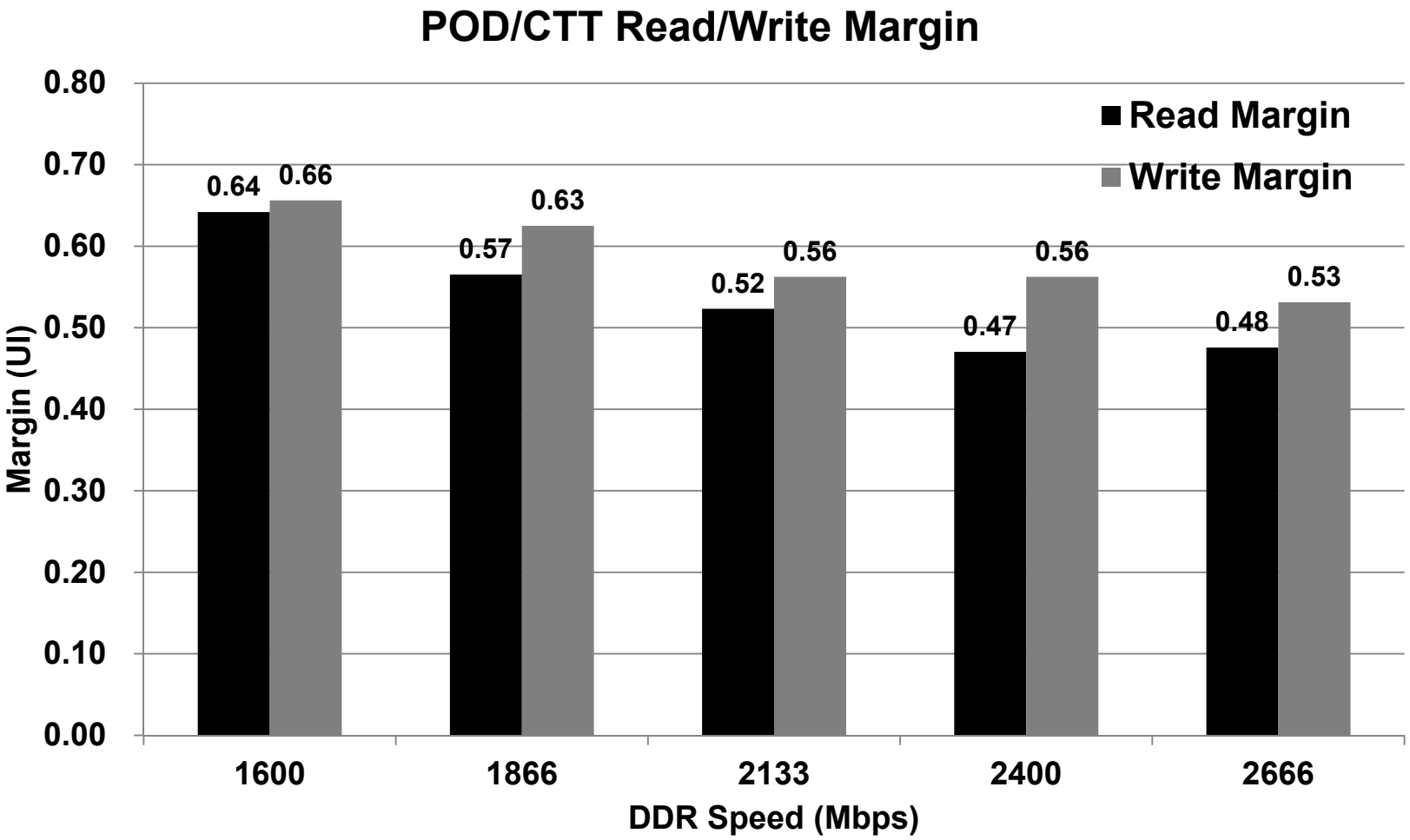
Developed Termination Topology



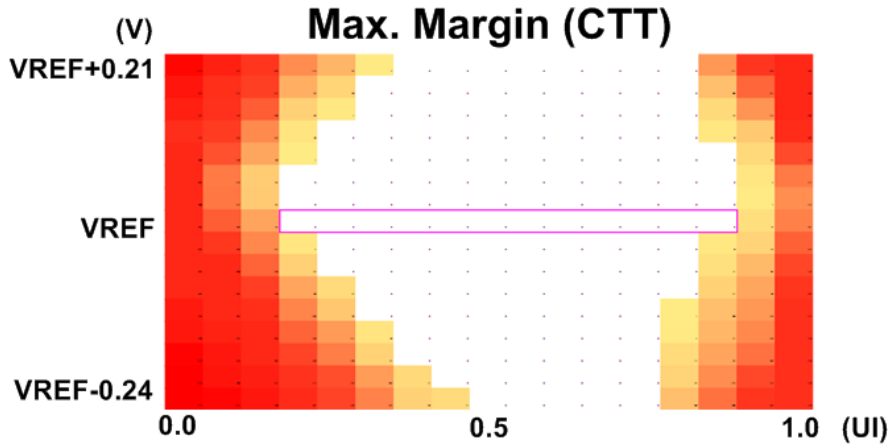
Measurement Results

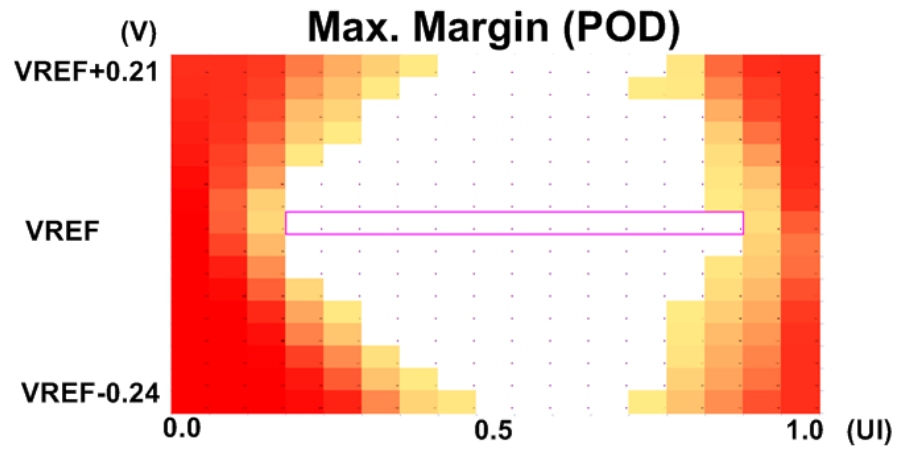


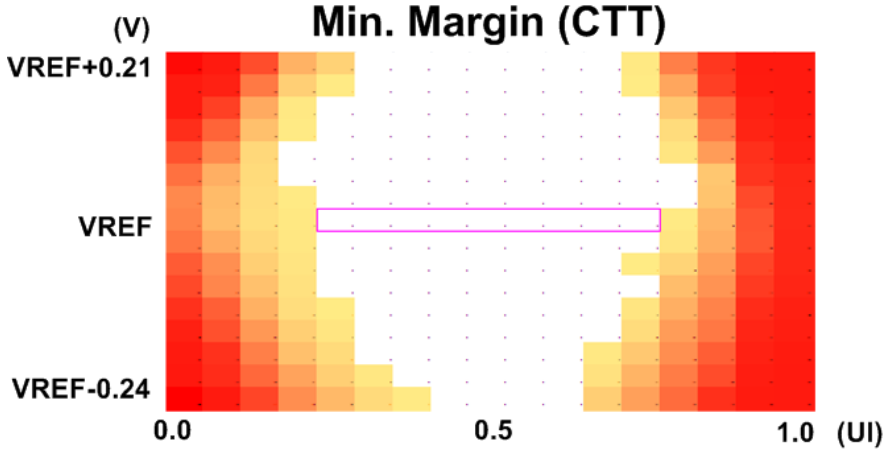
Measurement Results

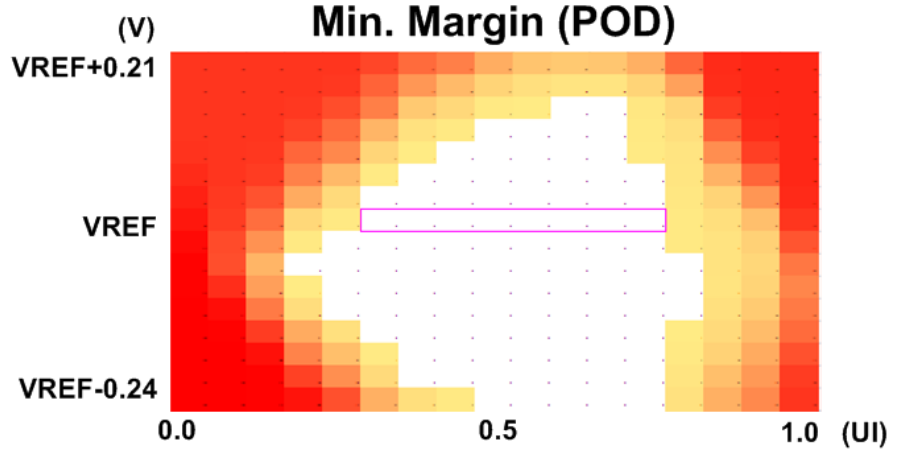


Measurement Results



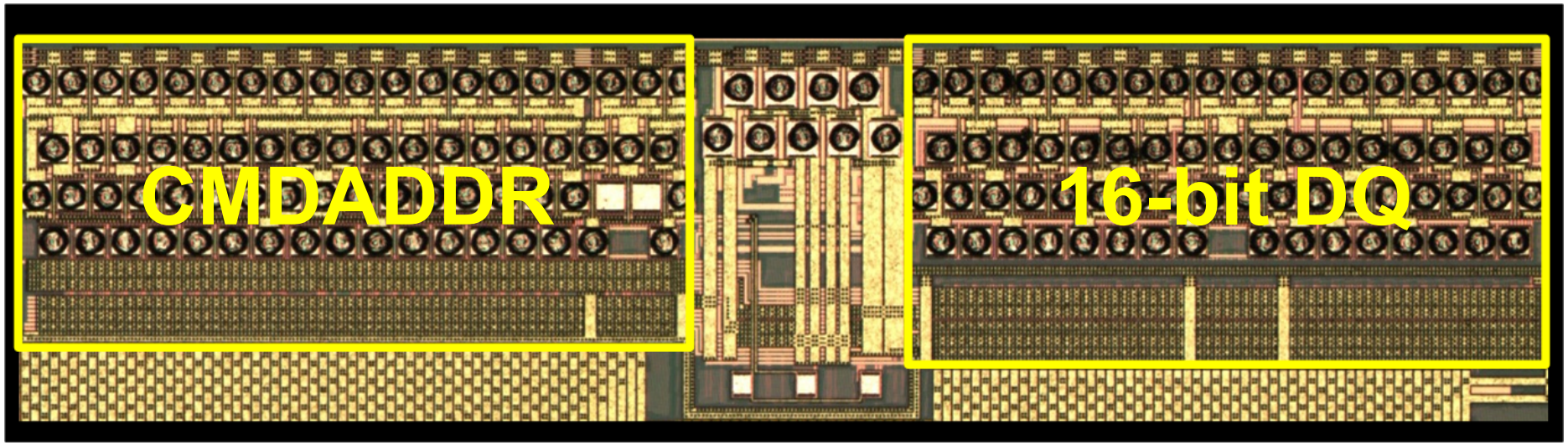






@2.667Gpb/s measured by internal eye monitor

Die Micrograph



40nm low power logic process

Summary

- Developed DDR3 memory interface
  - This DDR3 memory I/F can operate at 2.667Gbps on wirebond BGA package and single-end mounted PCB.
  - With asymmetric ODT, it can reduce around 125mA effectively when the system with 16-bit DDR3 interface operates in read operation.
  - Cost-effective solution

Reference

- [1] J. Feng, R. Schmitt, H. Lan, et al., “Signal and Power Integrity for a 1600 Mbps DDR3 PHY in Wirebond Package,” DesignCon, Feb. 2011.
- [2] R., Kumar, G. Hinton, et al., “A Family of 45nm IA Processors,” ISSCC Dig. Tech., pp. 58-59, Feb. 2009.
- [3] N. Kurd, S. Bhamidipati, et al., “A Family of 32nm IA Processors,” JSSC, pp. 119-130, Jan. 2011.